FEATURE ARTICLE

A Review of Three-Dimensional Resistive Switching Cross-Bar Array Memories from the Integration and Materials Property Points of View

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Issues in the circuitry, integration, and material properties of the two-dimensional (2D) and three-dimensional (3D) crossbar array (CBA)-type resistance switching memories are described. Two important quantitative guidelines for the memory integration are provided with respect to the required numbers of signal wires and sneak current paths. The advantage of 3D CBAs over 2D CBAs (i.e., the decrease in effect memory cell size) can be exploited only under certain limited conditions due to the increased area and layout complexity of the periphery circuits. The sneak current problem can be mitigated by the adoption of different voltage application schemes and various selection devices. These have critical correlations, however, and depend on the involved types of resistance switching memory. The problem is quantitatively dealt with using the generalized equation for the overall resistance of the parasitic current paths. Atomic layer deposition is discussed in detail as the most feasible fabrication process of 3D CBAs because it can provide the device with the necessary conformality and atomic-level accuracy in thickness control. Other subsidiary issues related to the line resistance, maximum available current, and fabrication technologies are also reviewed. Finally, a summary and outlook on various other applications of 3D CBAs are provided.

1. Introduction

As the scaling of a memory device proceeds down to the design rule of ≈10 nm, architectures with a vertically integrated structure (VIS) are attracting tremendous interest. This is because it is the most feasible method of continuously decreasing the cost/bit trend with increasing memory density. Another method of three-dimensional (3D) integration is stacking the two-dimensional (2D) memory array through either the chip- or cell-level stacking technology, but this may not be the economically viable method considering the astronomical cost of the fine patterning, which is necessary for each layer. In principle, VIS can alleviate this huge cost problem of multiple patterning, although it still faces many obstacles. Perhaps the most representative example of VIS is the bit cost scalable (BiCS) architecture suggested by Toshiba Company, Japan, several years ago, where the vertically aligned chains of charge-trap-flash memory cells comprise the 3D NAND memory cell array.[1] Due to the cost-effective fabrication processes involved in the VIS memory, various variations of the BiCS cell have been suggested and actively pursued.[2–5] These generally have a common problem, however: the channel, which corresponds to the bit line, is made up of semiconductors, either epitaxial single-crystal Si,[6] poly-crystal Si,[7] amorphous Si,[8] or even amorphous oxide semiconductors.[9,10] Of course, a semiconductor is necessary to make the flash-type memory cell, but these materials have inherently low carrier mobilities compared with metal, making the device operation speed inappropriate when the device scales <<15 nm of design rule. When the design rule reaches 10 nm, the allowed channel thickness is <≈5 nm; thus, the channel resistance could be too high to achieve reasonably fast memory operation even if the whole channel thickness is inverted. In addition, the statistical fluctuation of dopant concentration in such small semiconductor channel regions is another significant concern.[11]

Therefore, another technological breakthrough is necessary because the demand for higher-performance non-volatile memories (NVMs) will further increase in future electronic applications. Perhaps the only way to solve this problem is to use metallic word and bit lines. However, the electrical conductivity in metals can hardly be modulated by an electric field, unlike

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DOI: 10.1002/adfm.201303520

in semiconductors. One way to alleviate this problem is to use functional intervening layers consisting of resistance switching (RS) materials between the metal wires which are vertically integrated. This corresponds to the 3D modification of the well-known 2D crossbar-array (CBA) RS memory. However, various problems of the 2D CBAs, such as the sneak current problem,[12] could be retained or even aggravated in this structure if they are not appropriately addressed. With the L-layer stacking of CBA, the area for the memory cell can be decreased to $4F^2\ L^{-1}$, where F is the minimum feature size. If the RS has n different levels of resistance,[13–15] the memory cell area per data can in principle be further decreased to $4F^2\ (\log_2(n))^{-1}\ L^{-1}$. There are numerous problems, however, in realizing such an idealized memory, in addition to the very high cost for fabrication mentioned above.

One of the most notable problems of these passive-type array architectures is the presence of sneak current paths due to their extremely parallel geometry. **Figure 1** shows a schematic diagram of the typical 2D CBA, where the sneak current through the on-state neighboring memory cells (2, 3, and 4) disturbs the reading out of the off-state cell 1. In the worst case scenario, all the neighboring cells are in on-state, making the problem even more serious. Various methods have been suggested to solve this sneak current problem, such as incorporating diodes or any other types of highly nonlinear current-voltage (I–V) components in series with the memory cells.[16–28] Another problem is related to the resistance of the very narrow metal lines. The high line resistance in series with the RS memory cell adversely interferes with the RS itself as well as the high operation voltage and the accompanying power consumption.[29,30] Although metals have a much lower resistivity than semiconductors, which is why this issue has not been seriously considered, it actually bears serious problems in the highly scaled cross-bar-type memory. Nevertheless, the VIS memory has great advantages over 2D devices, as will be discussed in detail later.

The 3D-arrangement VIS cells, however, invoke a complicated problem related to the optimal placement of the periphery circuits to access each memory cell. If each layer requires its own periphery circuits, including sense amplifiers and decoders, the area required for the circuitry will overcompensate the area in the memory cell that had been saved by stacking for L values higher than a certain number.[31] In addition, the stacking of many layers, and their etching in the vertical direction, can be a big challenge in terms of fabrication, meaning that the adoption of VIS requires careful considerations of these various factors.

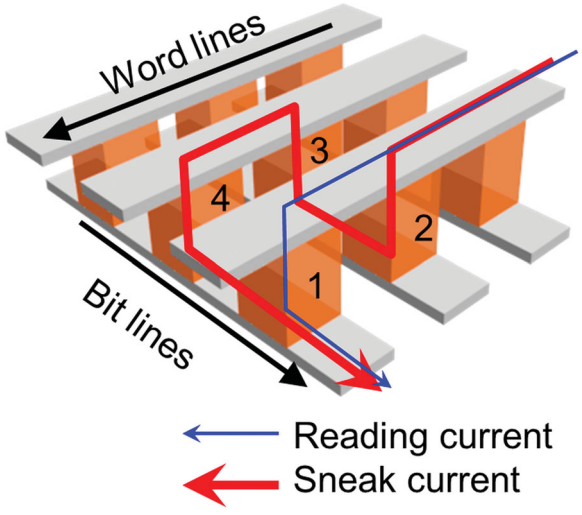

Figure 1. A schematic diagram of the typical 2D CBA showing the read disturbance problem by the presence of sneak current: reading current (thin blue line), sneak current (thick red line).

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Therefore, in this article, the authors attempted to review all the possible problems of CBAs with 2D and 3D configurations from the viewpoints of circuit and material properties. The recent progresses in addressing the key issues including the sneak current and the optimization of VIS in terms of the necessary numbers of bit lines, word lines, and contacts to address each memory element are also reviewed. In order to accomplish these goals, a general and easy way of understanding the complicated structure of the 3D memory array in terms of the total resistance of the sneak current paths is presented, which greatly facilitates the understanding of the material properties required for memory and selection devices. Several possible *I*–*V* characteristics of memory cells (including the characteristics of selection devices) are suggested, and their influence on the array performance is also discussed in detail. This work will provide the research field with general guidelines regarding the electrical characteristics that RS memory cells should have in CBA forms.

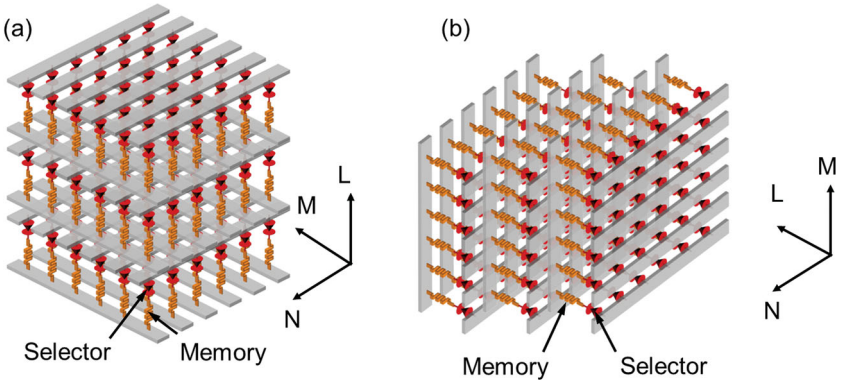

Figure 2. The standard structures of cross-line type 3D CBA: a) vertical stacking and b) horizontal stacking of 2D CBA.

According to the impending importance of the 3D CBA for next generation non-volatile memories, several works have been reported very recently.[32–36] However, those works addressed only certain specific aspects of the 3D CBA, which makes it necessary to publish a more comprehensive review on the material, processing, as well as circuit points of view in this field.

The discussion part of this review consists of several sections. The first two sections (Sections 2.1 and 2.2) deal with issues related to the 3D CBA structures in which the word and bit lines are in the form of wires. Then, the discussions are extended to 3D CBA structures with "word planes", which can largely decrease the necessary number of interconnection wires and circuit overhead (Section 2.3). Section 2.4 deals with the sneak current path problem mainly found in 2D CBA structures in a quantitative manner, and Section 2.5 describes the same problem in 3D CBA structures. Section 2.6 discusses various voltage bias schemes applied to word and bit lines for reading in CBA, and Section 2.7 discusses the problems related to the high resistance of word and bit lines when they become extremely narrow. Section 2.8 deals with the correlation between the characteristics of various selection devices and memory elements for forming the CBA structure, and Section 2.9 describes fabrication-related issues, such as the atomic layer deposition of relevant materials. Finally, Section 2.10 describes other miscellaneous problems that were not or partly dealt with in the other sections. Section 3 summarizes the discussions and provides outlooks of the CBA memory.

2. 2D and 3D CBA Structures; Wires, Selectors, and Memory Elements

2.1. Number of Interconnection Lines in the Cross-Line-Type CBA

First, the number of necessary interconnection lines (n_{il}) in the memory cell region for 2D and 3D CBAs are considered. It can be easily understood that n_{il} determines the number of total contacts as well as of the metal wires that connect the memory cells to the periphery circuits, so that minimizing n_{il} is as important as decreasing the memory cell size because contacts and interconnection wires take Si substrate area. In a 3D CBA, n_{il} is determined by the number of word lines (M), bit lines (N), and layers (L). In addition, each bit line has its own sense amplifier, which generally takes up a larger area, so that minimizing N is preferred over minimizing M for the given total number of cells (C). In general, the area of word line drivers is smaller than that of bit line drivers that include sense amplifiers.

There are several methods of stacking 2D CBA into 3D CBA. Among these, the simplest is just stacking 2D CBAs on top of each other, as shown in **Figure 2**a, while each 2D CBA is separated from each other by an insulating layer. In this article, this type of 3D CBA is referred to as "cross-line-type CBA". As this is just a repetition of 2D CBAs, C in a cross-line-type CBA is determined by the product of numbers of word lines, bit lines, and stacks, i.e., $C = MNL$. Thus, minimizing n_{il} in such a CBA for given C and L means minimizing $M+N$, and the minimum n_{il} is achieved when $N = M$. This can be more formally explained as follows: in the cross-line-type CBA, $n_{il} = (N+M)L$, and $L = C/(NM)$, so that $n_{il} = (N+M)(C/(NM))$. **Figure 3** shows the variation of n_{il} as a function of M and N (note that L is not an independent variable) for $C = 10^6$, i.e., a 1 Mb cross-line-type CBA. It can be easily understood that the condition of $M = N = 100$ results in a minimum n_{il} of 20 000, which is the number of total word and bit lines, implying that the numbers of contacts and interconnection lines to the periphery circuits are also 20 000. It is obvious that this cannot be the optimum architecture because this 3D CBA type hardly shows advantages over 2D CBAs in terms of n_{il}. Note that a 1 Mb 2D CBA requires an n_{il} of just 2000 ($M = N = 1000$).

Another important concern, apart from the aforementioned purely geometric consideration of the layout of the memory cells, is the difficulty in the fabrication of multiple layers in cross-line-type 3D CBAs. In the structure shown in Figure 2a, the number of lithographic processes is proportional to L; thus, increasing L to make the effective memory cell area smaller entails increasing the lithographic steps, which costs very much. Therefore, L should be regarded as an independent

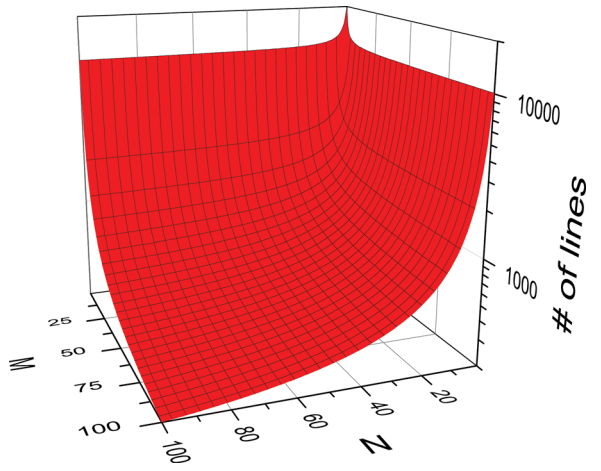

Figure 3. A three-dimensional representation of n_{il} as a function of M and N for the cross-line type CBA.

variable given by the difficulty and cost of 3D CBA fabrication, unlike the previous demonstration, where L was taken as a variable only depending on M and N. An alternative architecture can be seen in Figure 2b, where the structure shown in Figure 2a was simply rotated by 90° with respect to the axis of N (or M). In this case, the number of stacked layers becomes M (or N). Compared with the structure in Figure 2a, this type of structure requires a much smaller number of lithographic processes, which can decrease the fabrication cost by combining the deposition of the multiple layers with subsequent anisotropic etching of the whole layer stack in one step if the etching and subsequent functional layer deposition technologies are available. However, this structure leads to the following critical issue in terms of n_{il}. For instance, when the allowed number of stacked layers of a 1 Mb cross-line-type CBA is 10 due to the difficulty and high cost of fabrication, a minimum n_{il} of 6320 ($n_{il} = (N+M)L$; $N = M = 316$ and $L = 10$) can be achieved for the structure in Figure 2a. For the structure depicted in Figure 2b of the same density with $M = 10$, however, n_{il} is 100 010 because $N = 100\,000$ and $L = 1$ minimizes n_{il}. This is a questionable conclusion deriving from considering only the minimization of n_{il} for this structure. This, in fact, excessively increases the resistance of the bit lines and leads to an extremely high n_{il}. Therefore, careful optimization considering the geometry and the processing cost is required.

2.2. Further Optimization of the Cross-Line-Type CBA

There are several ways to solve or mitigate the problem of increasing n_{il} when the stacked-layer number of the cross-line-type 3D CBAs is increased. Among them, sharing the bit and/or word line between neighboring layers is an easily accessible method assuming the sequential writing and reading of the memory cells during the memory operation. Lee et al. suggested a shared-bit-line structure, as shown in **Figure 4**a, where one bit line serves two adjacent memory layers.[20] With this type of structure, the number of bit lines can be half of that of the structure shown in Figure 2a. A similar shared-line structure can also be considered for word lines. As each

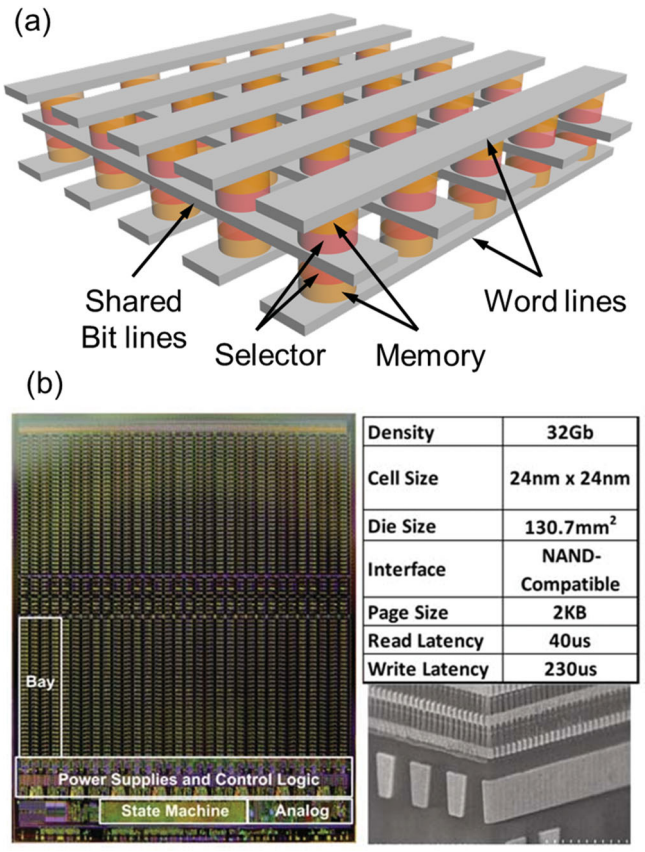

Figure 4. a) A schematic diagram showing the shared bit line structure in cross-line type 3D CBA. b) Optical microscope image of 32 Gb CBA using the shared bit line structure reported by Toshiba's and Sandisk's group (left panel). Summary of device features (upper right panel) and scanning electron microscopy image of two-layer stacked memory cells (lower right panel). Reproduced with permission.[37] Copyright 2013, IEEE.

bit line, however, is connected to a sense amplifier, the shared-bit-line structure is superior to the shared-word-line structure because the number of necessary sense amplifiers is smaller for the shared-bit-line structure, and, thus, the area taken up by the sense amplifiers is smaller. Toshiba's and Sandisk's group recently reported cross-line-type CBAs, in which each memory block was composed of 4k × 2k cells[37] (Figure 4b). They stacked two layers of such a CBA while adopting a shared bit-line structure, and achieved a memory density of 32 Gb per chip, which is the highest density CBA (or resistance switching random access memory (RRAM)) reported up to now. Figure 4b shows the layout of the 32 Gb CBA chip (left panel) summary of device features (upper right panel) and detailed images of a memory cell block (lower right panel). A more detailed structure of the memory cell with shared bit-line structure could be found from Figure 12.1.1 of ref. [37].

The same idea can be applied to the structure in which the bit lines direct vertically, as shown in **Figure 5**a.[38,39] Meanwhile, for the structure shown in Figure 5b, the necessary number of word lines is decreased to half of what is shown in Figure 5a. In this structure, two word lines are served by one word line driver, so that the circuit overhead is also decreased.[40] It must be noted that for these types of structures it is basically

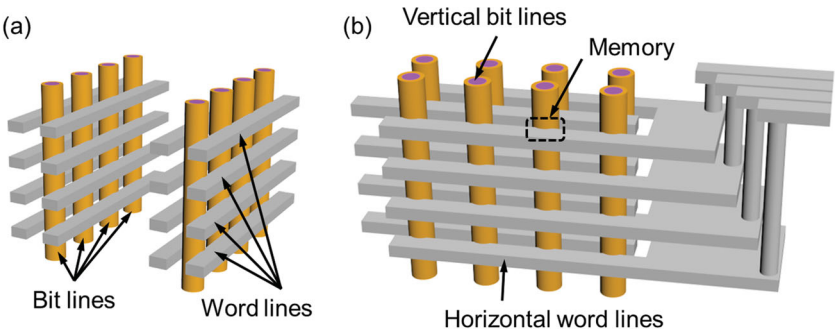

Figure 5. Schematic diagrams showing the shared bit line structure in cross-line type 3D CBA: a) a vertical shared bit line structure and b) a shared lateral word line and vertical bit line structure.

assumed that the RS layers do not conduct electricity along their surface direction; otherwise, the functional RS layer between the memory cells must be etched away, which is very difficult, especially in VIS. Sharing bit and/or word lines is possible because only one cell from a selected bit line is addressed at a certain moment of memory operation, with the help of bit and word line decoders. The issues related to the decoders will be discussed next.

Figure 6a,b show two basic strategies of building 3D CBA structures regarding the location of the periphery circuits with respect to the memory core region, where all periphery circuits are fabricated on a Si wafer surface and on each memory layer, respectively. An intermediate-type structure is also possible, i.e., relatively simply circuits, such as sense amplifiers, word line drivers, and decoders, are formed on each memory layer but more complicated and higher-performance logic circuits are to be formed on the Si surface. From the point of view of structural simplicity, Figure 6b is definitely better than Figure 6a or the intermediate structure because it greatly decreases the long and complicated layout of the metal wires that connect the memory cells and the periphery circuits. An immediate problem of the structure in Figure 6b, however, is that the aforementioned circuit elements, which are composed of mostly complementary metal oxide semiconductor field effect transistors (CMOSFETs), cannot be fabricated on a Si wafer.

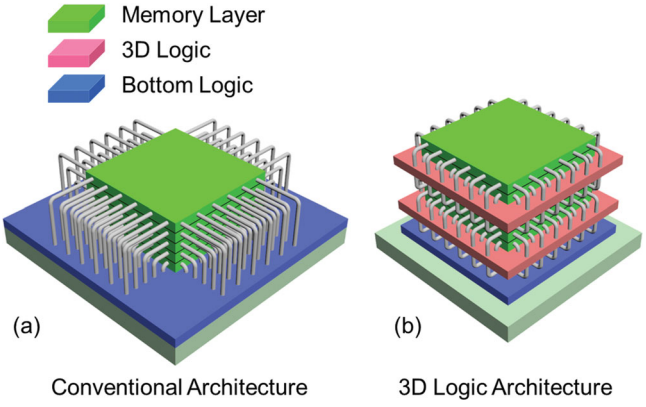

Figure 6. Schematic diagrams showing a) a conventional architecture with bottom logic circuit only and b) a 3D architecture using CMOS logic circuits placed at each memory layer.

There are currently no reliable fabrication technologies available for CMOSFET logic circuits that do not require the use of single crystal Si. The currently available circuit technologies using poly-Si,[41] amorphous-Si,[42] and even amorphous oxide semiconductors (AOSs), such as $InGaZnO_4$,[43] are not sufficiently advanced for fabricating high-performance digital circuits for memory applications. Furthermore, the highly reducing H_2 gas atmosphere at high temperatures (>≈500 °C) for poly- or amorphous-Si deposition is usually not compatible with oxide-based RS materials. Oxide-based RS materials are most likely to be severely degraded during those processes, resulting in even the malfunctioning of memory cells. In this regard, the recent progress in the AOS field appears quite notable, even though the present status is still far behind the state-of-the-art level of Si-CMOSFETs. The primary merit of AOSs is their low fabrication temperature (even at room temperature by sputtering) under oxidizing atmosphere, which minimally influences the performance of RS oxides.[43] The amorphous nature of AOSs fundamentally mitigates the problems related to the presence of grain boundaries in poly-Si. Their low carrier mobilities, however, which are generally several tens of $cm^2\ V^{-1}\ s^{-1}$, lower than that of single-crystalline Si by one order of magnitude, and the lack of stable p-type AOS thin-film transistors (TFTs), are the two big huddles that must be overcome.[44]

Nevertheless, there have been several impressive improvements in this field. Lee et al. reported AOS TFTs usable in the peripheral circuits of resistance switching random access memories in the one-transistor and one-resistor (1T-1R) configuration.[31,45] They also reported that the AOS TFTs have sufficient current drivability to induce stable RS operation.[31] The AOS TFTs were further integrated into logic circuits implementing NOT, NOR, and NAND functionalities, which is a very promising result in this field.[46] The reported device size, however, remains at a quite large scale (2 μm line width), and the lack of p-type AOS TFTs makes the circuit design, fabrication, and operation inefficient compared with those of the complementary-type circuits. Therefore, there must be tremendous improvements in this field for the AOS TFTs to be actually adopted in highly scaled memory devices. Meanwhile, AOS TFT circuits printed on glass substrates can be a viable option for high-performance display applications, where the miniaturization of TFTs is not a serious problem.[43]

Kügeler et al. suggested a different method to decrease the circuit overhead of 3D CBAs, using a device called "layer decoder".[47] Decoders allow only selected lines, among many parallel bit or word lines, to be connected to the periphery circuits outside. In a cross-line-type 3D CBA, each memory layer is a separate circuitry, meaning that the periphery circuits for each layer take up a large portion of the Si wafer surface area. According to the report by Küegler et al., the layer decoder decodes each memory layer just as the bit and word line decoders decode bit and word lines in a certain memory layer. Using the layer decoders enables the wafer surface area for decoders to be significantly decreased although the

(simultaneous) parallel access of different memory layers is sacrificed. In this structure, the layer decoders control switches (made of MOSFETs) that connect the column and row decoders formed on the Si wafer, which serve all bit and word lines in the 3D CBAs and the bit and word lines in all memory layers. With this structure, only one set of column and row decoders is necessary to decode all memory cells with the help of switching transistors. Therefore, the periphery circuits do not need to be increased with the increasing number of layers as shown in Figure 6a. This structure, however, has the following problems: First, switching transistors must be formed on each layer, meaning that part of the Si surface cannot be used for this purpose. Perhaps, a part of the RS memory cells can be used as the switching device for this purpose. Secondly, the connection wires between the bit and word lines and the layer decoders can be long and complicated. Third, the parallel access of different memory layers becomes impossible as mentioned above, so that the overall device operation speed decreases significantly.

Another 3D CBA memory array architecture has been suggested by Strukov and Williams.[48] The key feature of this architecture is the characteristic connection of word- and bit-lines among the many stacked layers, thereby all the memory cells within the 3D CBA structure are in fact equivalent to the folded 2D CBA structure. In this architecture, the word- and bit-lines in each stacked layer were cut into several pieces and shifted laterally to make the via spaces for vertical connections between the lines in different layers. With this characteristic structure, the folded word- and bit-lines, topologically lying on the 3D structure, could be controlled by one set of CMOS circuits fabricated on a Si wafer surface, which was located below the 3D CBA memory block. It was suggested that the physical location of the memory cells is mapped to a four-dimensional logical address space such that unique access from the CMOS substrate is provided to every memory cell in a stacked array of CBAs. It was also shown that such a structure could be the architecture in digital memories, field-programmable gate arrays, biologically inspired adaptive networks, and state-of-the-art integrated circuit foundries. Such a structure offers the possibility that 4 N lines can access a number of memory cells < N^2.

2.3. Word-Plane-Type CBAs

It was made clear above that decreasing n_{il} is of critical importance for improving the integration density of cross-line-type 3D CBAs. As n_{il} should be decreased in accordance with the decreased number of decoders, there is less consumption of the Si wafer surface area. Of even greater importance is the fact that a smaller n_{il} results in less complicated and shorter wires that three-dimensionally connect the bit and word lines to the periphery circuits.[46] A substantial decrease in n_{il} can be achieved when the so-called "word planes" are adopted instead of word lines, as shown in **Figure 7**a,b.[49,50] Such structures are called "word-plane-type 3D CBAs". In these structures, it is assumed that selection diodes serving as cell selectors, which are necessary to suppress sneak current, and RS memory cells are placed at the junction region between word planes and bit lines. In addition, the forward direction of a diode is set to be consistent with the current flow direction for writing and reading of a memory cell. As can be easily understood from Figure 7a,b, when one word plane is activated, all the cells on that word plane are ready to be accessed. However, only cells whose bit line is activated are addressed during writing and reading. Thus, the word plane structure works in this way if the sneak current is sufficiently low. The sneak current issue in this structure will be discussed in detail later, in comparison with 2D CBAs. As it is quite obvious that the required number of periphery circuits for this word-plane structure is much smaller (discussed in detail below), this structure is superior to the cross-line-type CBAs with respect to its higher cell efficiency (ratio of the volume taken by the memory cells to the total available volume) as well as its packing density because the space between neighboring word lines is no longer necessary.

Considering the general operation principle of matrix-type memories,[51] the "bit plane structure" appears to be possible as well. In this case, however, the operation speed becomes much slower than for the word plane structure because the columns (or rows) of word lines connected to a common word line decoder must be accessed one by one. By contrast, in the case of the word plane structure, the decoders for the columns (or rows) of bit lines that are connected to one bit line decoder would work simultaneously, so that the access speed could be much faster. Therefore, the word plane structure is preferred, even though the necessary space for sense amplifiers for each bit line could be large.

Regarding Figure 7a,b, the total numbers of word planes and bit lines, also called "n_{il}" here, is $(LN)+M$, and $L=C/(NM)$. Therefore, $n_{il}=C/M+M$, which becomes minimized when $M=\sqrt{C}$. In addition, as $M=C/(LN)$, $LN=\sqrt{C}$. As long as $LN=\sqrt{C}$ is satisfied, varying the values of L and N does not change n_{il}.

Because of the difficulty in making many layers along the vertical direction, the following issue must be considered,

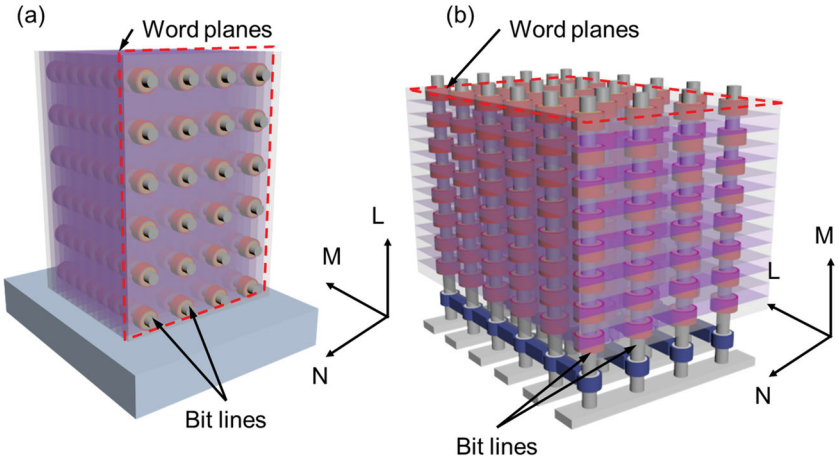

Figure 7. Schematic diagrams showing word-plane type CBAs: a) vertical stacking and b) horizontal stacking of word-planes.

however: L and M follow the vertical direction in Figure 7a,b, respectively. As mentioned earlier, the minimization of n_{il} requires the condition $M = LN = \sqrt{C}$ to be satisfied. In Figure 7a, this can be easily accomplished by increasing M and N, even when L is limited to a small number, such as 10. For this structure, when $C = 10^6$ and $L = 10$, the optimized structure in terms of n_{il} can be achieved when $N = 100$, $M = 1000$, giving a value of 2000 for n_{il}. This structure is quite flexible for achieving the minimum n_{il}, when varying L because of the limits for the process issues related to M and N are not severe.

In the structure shown in Figure 7b, however, the $M = LN = \sqrt{C}$ condition can hardly be satisfied because M is now the number of stacked layers. For instance, if M is assumed to be 10, as in case of Figure 7a, $N = L = 316$ gives the minimum n_{il}, but this actually results in a minimum n_{il} of 99 866, which is an excessively larger number compared with the other case.

Meanwhile, the structure shown in Figure 7b has a certain advantage over that in Figure 7a regarding the fabrication. In Figure 7a, the stacks of laterally aligned metal wires (bit lines) must first be fabricated followed by sequential formations of RS and selection devices (e.g., diode) onto the bit lines. Then, word planes are fabricated. Fabrication of free-standing metal wires is already quite challenging in this structure. In contrast, the structure shown in Figure 7b is much more favorable for fabrication because the word planes (e.g., metal) and insulating layers are alternatively deposited. Then, vertical holes are formed by anisotropic etching, and the RS and selection device layers are deposited sequentially. Finally, the holes are filled with the bit line material (metal). This is a much easier process than the other one, although the vertical etching of the bit line holes in the alternatively stacked layers is still challenging. Therefore, there have been several suggestions for mitigating the excessively large n_{il} problem of this structure, and one of the notable ones is discussed in the following.

The basic idea is to add an active matrix plane made of vertical transistors, indicated by the dark blue color in Figure 7b, which enable random access to the NL bit lines.[50] In this case, the number of wires that connect the bit lines decreases from LN to $L+N$, resulting in a drastic decrease of n_{il} from $LN+M$ to $L+N+M$. While n_{il} reaches its minimum when the condition $N = L = M = C^{1/3}$ is satisfied, the minimum n_{il} is practically achieved when $N = L = C/M$ because M is limited to a relatively small number due to the fabrication issues. In addition, the active matrix itself adds up the $N+L$ lines to n_{il}.

Meanwhile, word-plane-type 3D CBAs could have the drawback of capacitive coupling between the neighboring word planes, which are differently charged if the inter-plane dielectric layer is thin or has a high dielectric constant. Such capacitive coupling is generally seen in parallel metal wires in 2D devices, such as parallel bit lines in dynamic random access memories, but this effect could be further aggravated in structures having parallel metal planes. When the capacitive coupling is too large, the related RC delay could become very large and induce writing/reading operations. Therefore, the distance between the word-planes must be as long as possible or low-k dielectrics must be adopted. However, a too large distance results in an excessive increase in the height of the 3D stacked structure, which makes bit-line hole etching and film deposition challenging. Therefore, issues regarding both performance and fabrication must be considered.

2.4. Calculation of the Sneak Path Resistance in 2D CBAs

Next, the sneak current problems in 2D and 3D CBAs will be addressed. As discussed briefly in Figure 1, the extremely parallel and passive geometry of CBAs inherently induces unwanted leakage paths, which severely disturb the reading operation of a selected memory cell, especially, if it is in the off-state. The simplest case is shown in Figure 1, but it can be easily anticipated that there could be many other complicated situations where the sneak current contributes to the reading current or voltage. The leakage increases the power loss during the writing, and in some cases, an unwanted disturbance in the resistance states can even be induced. This type of problem is hardly encountered in devices employing a MOSFET as the selection device for each memory cell, such as dynamic random access memories or 1T-1R RRAM. The extremely nonlinear drain current versus gate voltage characteristics of MOSFETs can efficiently isolate selected cells from the neighboring cells when they are written or read out. In CBAs, however, MOSFETs can hardly be adopted as the selection device; as such, the sneak current issue is one of the most significant problems in this memory array structure.

In the following, a method to simplify and evaluate the complicated parallel sneak paths is provided, and methods to suppress the sneak currents, which have been suggested up to now, are summarized depending on the operation schemes of the RS memory cells in the subsequent sections. To begin with the simplest case, a 2D $N \times M$ CBA is considered, where N and M refer to the numbers of bit and word lines, respectively (**Figure 8**a). In Figure 8a, there are $(N-1)(M-1)$ sneak current paths (one of them is shown as the blue dashed line) when the cell represented by the red line is supposed to be read. To understand the circuit feature of such multiple leakage paths, one leakage path is chosen, and the current flow through the path is traced. Here, for the sake of simplicity, the resistance of the interconnection lines is ignored, but its influence is dealt with in Section 2.7. One can easily understand that each sneak path contains three sneak resistance components (R_{s1}, R_{s2}, and R_{s3}, shown in Figure 8a along the dashed blue line) while all other paths containing, for example, five R_s do not need to be considered because no current flows through the additional fourth and fifth components as the electric potential drops across them are zero (as long as the line resistance is ignored). One example of five R_s is shown in Figure 8a for the green dashed line. The worst case scenario for the sneak current is that all memory cells are in on-state except for the selected cell, which is about to be read out. In this situation, for the sneak path shown in Figure 8a, the sneak current originating from the selected word line, flows into the bit line through one of the (N–1) R_{s1}, and then flows into another word line through R_{s2}. The current finally flows into the selected bit line via R_{s3}. This situation can be well represented by the equivalent circuit shown in Figure 8b. For a selected word line, the number of the cells, unselected but sharing the word line, is $N-1$, meaning that the sneak current from the selected word line is

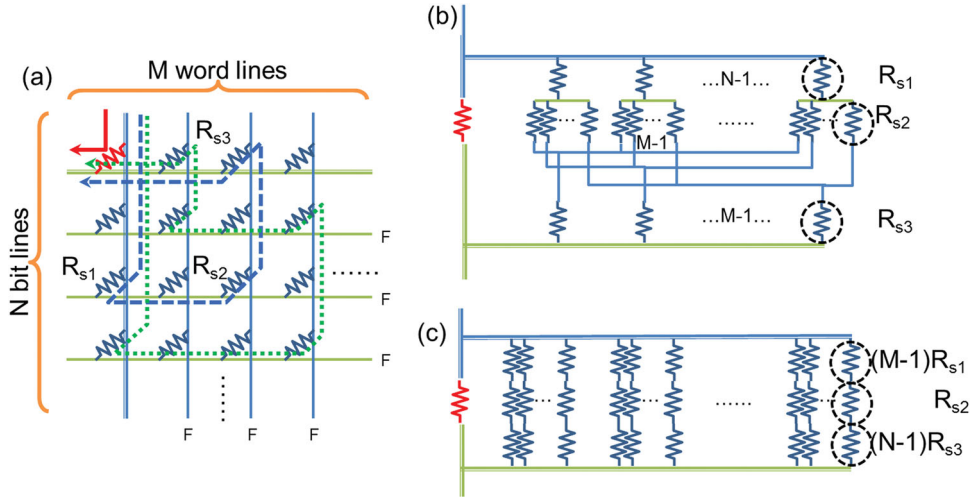

Figure 8. Schematic circuit diagram to explain the equivalent circuitry of 2D CBAs: a) circuit diagram of the 2D CBA reading current (red line); possible sneak path (blue long dashed line); impossible sneak path (green short dashed line), b) intermediately transformed circuit diagram, and c) finally transformed circuit diagram equivalent to that in (a). In (c), each sneak path is composed of serially connected $(M-1)R_{s1}$, R_{s2}, and $(N-1)R_{s3}$, and the total number of such sneak paths is $(N-1)(M-1)$. F represents floating.

divided into $N-1$ paths when it flows through R_{s1}. Each of the current components that just passed through the $N-1$ paths is divided again into $M-1$ paths when it passes through R_{s2}. Therefore, it can be understood that the total number of R_{s2} is $(N-1)(M-1)$, which is identical to the total number of sneak paths in the 2D CBA case. Finally, the $(N-1)$ sneak paths behind R_{s2} are connected to one of the $(M-1)$ R_{s3}, and the sneak current flows into the sense amplifier via the selected bit line. In this case, it can be noted that each R_{s2} is flown through by only one sneak current component while others (R_{s1} and R_{s3}) are flown through by certain sums of the variously divided current components. This can be understood from a slightly different point of view as follows: There are $(N-1)(M-1)$ sneak current paths in total (number of R_{s2}), which are connected to $(N-1)R_{s1}$ on the one hand and to $(M-1)R_{s3}$ on the other hand. This means that one R_{s1} is connected to $(M-1)$ paths, and one R_{s3} is connected to $(N-1)$ paths. The structure of one R_{s1} connected to $(M-1)$ paths is equivalent to the structure where $(M-1)$ numbers of $(M-1)R_{s1}$ are in parallel connection with each other. Therefore, the one R_{s1} can be represented by $M-1$ parallel connections of $(M-1)R_{s1}$. There are $(N-1)$ numbers of $\{(M-1)$ parallel connections of $(M-1)R_{s1}\}$, so that the number of $(M-1)R_{s1}$ in total is $(N-1)(M-1)$ in the equivalent circuit. A similar idea can be applied to R_{s3}: each R_{s3} has $(N-1)$ paths connected to it so that one R_{s3} can be represented by $(N-1)$ parallel connections of $(N-1)R_{s3}$. There are $(M-1)$ numbers of $\{(N-1)$ parallel connections of $(N-1)R_{s3}\}$, so that the total number of $(N-1)R_{s1}$ is $(M-1)(N-1)$ in the equivalent circuit. These are equivalent to the case where each R_{s2}, whose number is $(N-1)(M-1)$, is connected to $(M-1)R_{s1}$ and $(N-1)R_{s3}$, which can be represented by the equivalent circuit diagram shown in Figure 8c. Now, it can be understood that a parasitic circuit composed of $(N-1)(M-1)$ parallel resistors, with each resistor consisting of serially connected $(M-1)R_{s1}$, R_{s2}, and $(N-1)R_{s3}$, is connected to the selected memory cell represented by the red color, as shown in Figure 8c. Then, the overall resistance of all sneak paths (R_{st}) can be easily calculated using Equation (1).

$$R_{st} = \frac{R_{s1}}{N-1} + \frac{R_{s2}}{(N-1)(M-1)} + \frac{R_{s3}}{M-1} \quad (1)$$

It also has to be noted that the sneak current flows from the word to the bit lines through R_{s1} and R_{s3} while for R_{s2} it is the other way around. This has important implications when unidirectional selection devices, such as diodes, are implemented, as will be discussed later. A similar idea to understand the parasitic resistance of CBAs has been suggested by Flocke and Noll.[52]

2.5. Calculation of the Sneak Path Resistance in 3D CBAs

The idea for calculating R_{st} in 2D CBAs can be extended to 3D CBAs, as will be discussed in the following. As discussed in detail in Sections 2.2 and 2.3, there could be two representative types of 3D CBAs: the cross-line-type and the word-plane-type. It is quite obvious that R_{st} for the cross-line-type 3D CBAs must be identical to that in Equation (1) because each layer is isolated from each other, so that they are completely independent, meaning that R_{st} is completely independent of L.

For the word-plane-type 3D CBAs, however, the number of the bit lines connected to one word plane is much larger than in the other case, so that the number of sneak current paths increases accordingly. Fortunately, the formulation of R_{st} for the word-plane-type 3D CBAs can be easily accomplished by considering that the number of the bit lines connected to one word plane is NL, which is equivalent to the situation where there are NL connected bit lines per one "equivalent" word line. This means that N in Equation (1) can be replaced by (NL), leading to Equation (2) for R_{st} of the word-plane-type 3D CBA.

$$R_{st} = \frac{R_{s1}}{NL-1} + \frac{R_{s2}}{(NL-1)(M-1)} + \frac{R_{s3}}{M-1} \quad (2)$$

This means that the overall R_{st} becomes smaller when L increases in this type of structure, while no influence of L on R_{st} in the cross-line-type 3D CBA can be found. This is one of the crucial drawbacks of the word-plane-type 3D CBAs. It has to be kept in mind, however, that n_{il} can be smaller when a word plane is used instead of word lines. Therefore, there is a trade-off between n_{il} and R_{st}, as shown below. **Figure 9** shows the variation in the ratio of n_{il} and R_{st} between cross-line-type and word-plane-type 3D CBAs as a function of L, where the values for the cross-line-type 3D CBA were taken as reference. Here, it was assumed that $N = M = 100$, $R_{s1} = R_{s3} = 100\ \Omega$, respectively. It was further assumed that diodes with a rectification ratio of 10^7 were adopted, meaning that $R_{s2} = 10^9\ \Omega$. The R_{st} ratio of the word-plane type 3D CBA decreases rapidly with L; for instance, at $L = 10$, the R_{st} ratio decreases down to ≈10% R_{st} of the cross-line-type 3D CBA, while the n_{il} ratio decreases only by ≈50%. This is a highly undesirable situation for the word-plane-type CBAs. However, R_{st} of word-plane-type CBAs is still more than 10 000 Ω, which is enough to prevent read disturbance with 100 kbits cells. Although the R_{st} ratio decreased significantly compared to the cross-line-type CBA, adopting a higher performance diode is effective.

It should be noted that Equation (2) is valid for the basic 3D CBA structure while the modified version of 3D CBA, such as the shared-bit-line structure, requires a further modification of the equation. In general, at a given C, decreasing n_{il} by any means corresponds to increasing the number of the cells sharing one line (bit line, word line, or word plane). This is represented by the increases of N, M, and L in Equation (2) so that decreasing n_{il} to increase the cell efficiency necessarily increases the sneak current. Therefore, tighter specifications are required for the cell selection devices, as discussed in detail in Section 2.8. An issue closely related to the sneak current problems is the voltage application scheme for reading out the data, which will be discussed next.

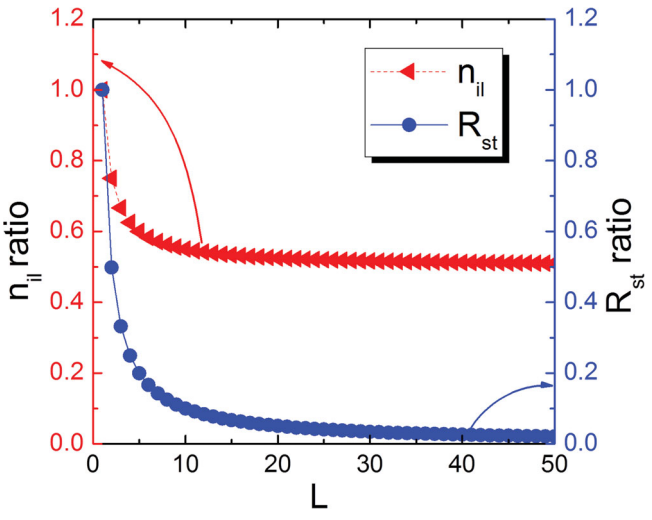

Figure 9. Variation in the ratio of n_{il} and R_{st} between cross-line type 3D CBA and word-plane type 3D CBA as a function of L, where the values for cross-line type 3D CBA were taken as reference, when the rectification ratio is 10^7, $R_{s1} = R_{s3} = 100\ \Omega$, and $N = M = 100$.

2.6. Bias Schemes for Reading in CBAs

There are various schemes of voltage application that can be used in CBAs to read out the data, and four of the typical ones are shown in **Figure 10**, where V_r is the read-out voltage. The primary reason for the presence of various voltage application schemes is to decrease the sneak current for a given CBA structure. Secondly, a certain type of selection device requires a specific voltage scheme, as discussed below.

The writing and erasing operations can be considered in the same way as the reading operation except for the fact that higher set and reset voltages than the read-out voltage are applied to the selected memory cell. Much lower voltages are applied to all unselected memory cells, so that the writing/erasing disturbance is much less severe than the reading disturbance due to the presence of sneak current paths. Therefore, only problems related with the reading are dealt with in this article.

The voltage schemes shown in Figure 10 can be classified according to the voltages applied to the unselected bit and word lines while the selected cell always has V_r applied to it when the data in it is read out. Figure 10a shows the simplest voltage scheme, where the word and bit lines connected to the selected cell are biased to V_r and 0 V, respectively, while all the unselected lines are floated. This bias scheme is referred to as "V_r scheme" in this article. The three neighboring cells included in the dotted line in Figure 10a constitute one sneak current path, where the voltage drop over these three cells is V_r. This scheme coincides with the simplest case when the data in the selected cell is read out, so that the circuitry for this scheme could be simpler than that of the other schemes. The second voltage scheme is shown in Figure 10b, where the difference from that shown in Figure 10a is that $V_r/2$ is applied to all the unselected lines. In this case, the cells sharing selected word and bit lines are biased to a voltage of $V_r/2$ while all the other cells connected to the unselected lines are biased to 0 V. This is called "$V_r/2$ scheme". In this scheme, R_{s1} and R_{s3} show a voltage of $V_r/2$. A similar voltage scheme adopts voltages of $V_r/2$ and $-V_r/2$ applied to the selected word and bit lines while all the unselected lines are connected to the ground ($-V_r/2$ scheme). In this case, the memory cells sharing selected word and bit lines come to have $V_r/2$ and $-V_r/2$ voltages, respectively, while all the other cells connected to the unselected lines have 0 V. This is called "$-V_r/2$ scheme", which is similar to the $V_r/2$ scheme, except for the fact that the voltage of all lines becomes lower than in the case of the $V_r/2$ scheme by $V_r/2$. In the third voltage scheme, shown in Figure 10c, the unselected lines with $V_r/2$ in Figure 10b were now biased to $2V_r/3$ (column) and $V_r/3$ (row), which is called "$V_r/3$ scheme". The primary difference between the $V_r/2$ and $V_r/3$ schemes is that the maximum voltage on the unselected node is $V_r/3$ in the $V_r/3$ scheme while it is $V_r/2$ in the $V_r/2$ scheme, so the risk of unwanted sneak current is largely decreased in the former case. However, the circuitry for having $V_r/3$ is generally more complicated compared with that for having $V_r/2$. In the fourth voltage scheme, shown in Figure 10d, the selected word and bit lines are biased to V_r

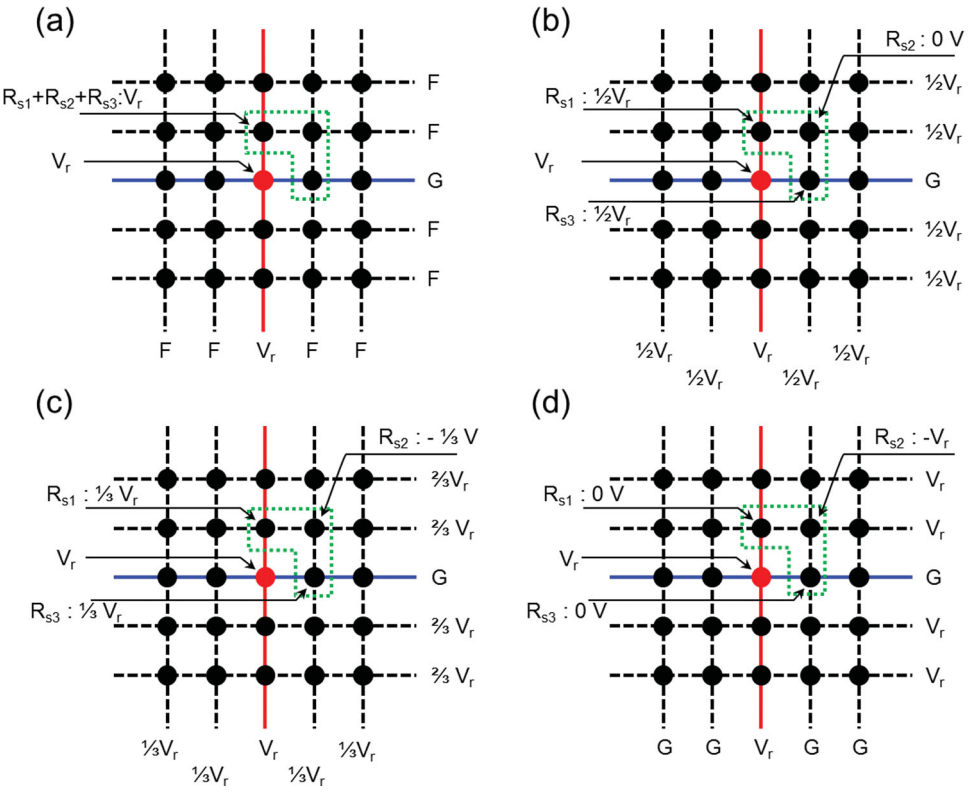

Figure 10. Four of the typical reading schemes for voltage application to word and bit lines: a) V_r scheme, b) $V_r/2$ scheme, c) $V_r/3$ scheme, and d) $-V_r$ scheme. G and F represent ground and floating, respectively. The $-V_r/2$ scheme adopts voltages of all lines being lower than in the case of the $V_r/2$ scheme by $V_r/2$. $-V_r/3$ scheme could be considered in a similar manner.

and 0 V, respectively, whereas all the unselected word lines are grounded and all the unselected bit lines are biased to V_r. This is called "$-V_r$ scheme". With this voltage scheme, only the cells sharing the selected word and bit lines come to have 0 V while all the other cells have $-V_r$.

Table 1 summarizes the voltages applied to the resistance nodes (R_{s1}, R_{s2}, and R_{s3}) of any arbitrary sneak path for each voltage scheme. As mentioned above, any arbitrary sneak path is constituted by the three series components, R_{s1}, R_{s2}, and R_{s3}, so that by considering the sneak current the voltage distribution among the three resistance components is conceived irrespective of the types of voltage application schemes. The selected cells must have V_r irrespective of the voltage schemes. This table allows one to easily determine what type of selection device must be adopted to block out the large sneak current. For example, in the $-V_r$ scheme, $-V_r$ is applied to R_{s2}, while a voltage of 0 V is applied to R_{s1} and R_{s3}, which renders diode-type selection devices highly desirable for this case. In contrast, it can be understood that the diode-type selection devices cannot be adopted for the $V_r/2$ and $-V_r/2$ schemes because the bias polarity of R_{s1} and R_{s3} are identical to that of the selected cell voltage, for which reason rectification will not work. It could be conceived that a diode can provide not only rectification but also non-linearity in the forward bias region, which could be useful to suppress the read disturbance further. However, as aforementioned, almost all the voltage drop along the sneak path is made at R_{s2}, which is the reverse diode node, so that there is no need for the non-linearity for the other nodes. In fact, the forward current of the diode should be as high as possible even at very low voltage in order to not disturb the memory operation which usually requires high current flow. Therefore, in fact, the non-linearity in forward direction is an unwanted aspect of a diode.

Table 1. The voltage applied to the resistance nodes for the four types of reading schemes discussed in Figure 10.

	Selected Cell	R_{s1}	R_{s2}	R_{s3}
V_r scheme	V_r	V_r over three terms		
$^1/_2V_r$ scheme	V_r	$^1/_2V_r$	0	$^1/_2V_r$
$^1/_3V_r$ scheme	V_r	$^1/_3V_r$	$-^1/_3V_r$	$^1/_3V_r$
$-V_r$ scheme	V_r	0	$-V_r$	0

As discussed in detail in Section 2.8, there are typically two types of selection devices: the rectifier, such as the diode, and the devices with a highly nonlinear *I-V* characteristic (a very low current at $V_r/2$, with a several orders-of-magnitude higher current at V_r). The former utilizes the rectifying function of the diodes and is thus appropriate for the cases when (R_{s1}, R_{s3}) and R_{s2} have opposite bias polarities applied to them. The latter is appropriate when the three resistance components have different absolute voltages applied to them, but with the same polarity.

In the V_r scheme, V_r is applied to the sum of R_{s1}, R_{s2}, and R_{s3} and the value of each term depends on the voltage drop over each. In this scheme, both diodes and nonlinear devices can be used. In the case of the diodes, almost all the V_r is applied to R_{s2} because R_{s2} is in the reverse direction while R_{s1} and R_{s3} are in the forward direction for the given V_r condition. Thus, the higher the reverse-direction resistance of the diode is, the smaller the sneak current is. When the nonlinear I–V devices are adopted, the voltage drop over the R_{s1} and R_{s3} components becomes larger than that over the R_{s2} component because the denominator $(N-1)(M-1)$ of the R_{s2} component is much larger than those of the other two (see Equation (1), meaning that R_{s2} becomes much smaller than those of the two other terms. In this case, the higher the nonlinearity is, the smaller the sneak current is.

Applying voltages to the unselected lines can help to reduce the sneak current that undesirably contributes to the sensing signal, as in the cases shown in Figures 10b. The most characteristic feature of the $V_r/2$ and $-V_r/2$ schemes is that the voltage drop across R_{s2} is always zero, meaning that there should be no current across R_{s2}. This means that the sneak current that passes through R_{s1} flows out to the $V_r/2$ source in Figure 10b via the unselected bit lines, making the power consumption higher than that of the V_r scheme. For these cases, therefore, the sneak current contributing to the sense amplifier is the current originating from the unselected word lines to the selected bit line via R_{s3}. As the voltage bias directions of the read-out cell (selected cell) and the cell of R_{s3} are always identical (only the magnitudes are different), the diode-type selection devices cannot be adopted in this case; only the nonlinear I–V devices can be used. In practice, however, there is always a slight voltage drop over each line element due to the finite resistance of the fine metal wires, making the voltage over R_{s2} non-zero albeit much smaller than $V_r/2$. Therefore, the leakage current from R_{s1} to R_{s3} via R_{s2} cannot be completely disregarded, especially when the nonlinearity devices have a low current ratio between V_r and $V_r/2$. This effect is even more important in the $-V_r$ scheme. As can be understood from Table 1, the voltages over R_{s1} and R_{s3} are ideally zero, suggesting that this scheme is in principle completely free from the sneak current problem. On the other hand, R_{s2} has an applied voltage of $-V_r$, suggesting that there could be immense power loss due to the simultaneous current flow from the unselected bit lines (biased to V_r) to the unselected word lines (grounded). In addition, the small but finite voltage drop across the interconnection lines makes the voltages over R_{s1} and R_{s3} and the consequent sneak current non-zero. Adopting diodes can be a feasible solution to these problems because the voltage directions along the selected memory cells and R_{s2} are opposite while the nonlinear I–V devices have little relevance in this case as there are no nodes with a voltage of $V_r/2$. The authors carried out a significant modeling work for such a case elsewhere, considering all the possible leakage current paths and voltage drops not only over the memory cells but also over the metal line components.[19] For a 100 Mb block, a forward/reverse current ratio as high as $\approx 10^7$–10^8 is necessary for a diode to appropriately serve as the selection device. Also reported were experimental results on the Schottky-type metal/oxide junction diodes using the Pt/TiO_{2-x}/Ti junction structure.[53] This structure showed a rectification ratio of $\approx 10^6$ and proved to work as a fluent selection device in 2D CBAs.[54] In fact, the highly nonlinear characteristics of the Schottky-type diode also provided the CBA with noise protection functionality during the data retention test.[54]

The four reading schemes shown in Figure 10 basically read out the current. In contrast, the all-line pull-up scheme, which was described in detail in ref. [30,47], detects voltages utilizing the voltage divider to maximize the reading margin. In this scheme, the data could be read out from the voltage ratio between the pull-up resistor and selected cell. For this read operation, the selected word line was grounded and the selected bit line was charged with the pull-up voltage. In this case, there could be different reading margins depending on the bias conditions where the unselected word lines and bit lines are charged with different voltages. For the voltage read scheme, maximum reading margin could be obtained when all the unselected word lines and bit lines are charged with V_r.[29,30,52]

2.7. Influence of Line Resistance

Metal wires have been regarded as having negligible resistance in the CBA-type structure, but this is not the case when F shrinks down to the 10 nm scale. For example, assuming that the metal has a 10 μΩ cm resistivity and that the line exhibits a 10×10 nm^2 cross-section and a 2 μm length, which corresponds to a 1 Mb 2D CBA array (1000×1000 cells) with a design rule of 10 nm, the line resistance is as high as 2 kΩ, which is not negligible. Therefore, the worst-case RS cell, whose location is at the opposite corner from the voltage source, can have a series resistance as high as 4 kΩ, which is large enough to interfere with the RS operation of the memory cell if its overall resistance is not much higher than the series resistance. If the same 1 Mb memory consists of a 3D CBA with a $100 \times 100 \times 100$ arrangement, however, the maximum line length is 0.6 μm, and the maximum series resistance is 0.6 kΩ, which is ≈7 times lower than in the previous case. This could be another crucial merit of the 3D CBAs compared with the 2D CBA structure. The increased number of interconnection lines, however, is a drawback of such a structure, as discussed earlier.

When the metal wire resistance is too high, two serious problems are expected: interference of the RS memory operation and deviation of the sneak current from the expectation based on Figure 10 and Table 1, as has already been mentioned. For the adverse interference of metal line resistance, Kim et al. reported a detailed study on this issue for the case of the unipolar-type RS (URS) memories.[29] In a URS memory cell, the reset voltage is generally lower than the set voltage. One may consider a serial circuit consisting of one variable resistor, the URS memory cell, and another fixed resistor, the line resistance in this case, whose resistance is comparable to the on-state resistance of the URS memory cell. For a simple explanation, the reset and the set voltages are assumed to be 1 and 2 V, respectively, and the on-state resistance of the URS memory cell and the line resistance are commonly 100 Ω, and the system is required to switch from the on- to the off-state. When a voltage of ca. 2.5 V is applied to the serially connected resistors, the URS memory cell initially experiences 1.25 V, which is large enough to change the on-state to off-state. Immediately

after the occurrence of this change, however, almost all the applied voltage is transferred to the memory cell due to the much higher resistance of the off-state URS cell compared with the series line resistance. As this voltage is higher than the set voltage (2 V), it subsequently switches to the on-state, meaning that memory reset becomes improbable.[29] Therefore, the resistance of the line should be much smaller than the resistance of the on-state URS memory cell.

The various reading schemes discussed in Section 2.6 are based on the assumption that the line resistance is zero, which is actually quite inappropriate in CBAs at the nanometer-scale. The most significant problem related to the non-zero line resistance results from the fact that the small voltage is actually applied over the nodes where the voltage is supposed to be zero. Therefore, the nodes that are not supposed to conduct sneak currents actually conduct a slight sneak current. Further complications originate from the fact that the actual resistance from the voltage source or sense amplifier (or the specific decoder) to the selected cell varies in a wide range in a cell-by-cell manner, which makes the quantitative estimation of the total resistance very difficult. It must be noted that according to Equations (1) and (2) zero line resistance is assumed.

Increasing the metal line thickness allows the modeling presented in this work to have a higher applicability since the line resistance decreases. Under this circumstance, the suggested selection devices, the diode and the nonlinear *I*–*V* device, will minimize the interference or sneak current effects. Nevertheless, there are several reports addressing issues related to the finite line resistance. As mentioned in Section 2.6, the CBA circuit shown in Figure 10d ($-V_r$ scheme) was extensively studied using mathematical formulae derived from the basic Kirchhoff's law;[19] the voltage drop between one node and another node is independent of the intervening circuitry as long as there is no additional voltage source involved. This is a feasible method to consider the voltage drop across the interconnection line elements as well as the memory nodes, but the problem with this method is that it is not incorporated into the standard simulation package.

Liang and Wong worked on the $-V_r/2$ scheme (to make it also applicable to the $V_r/2$ scheme) of 2D CBAs.[55] They assumed that the resistance of each line component connecting the neighboring cells is 1.25 Ω, which is a reasonable number, and calculated the read voltage margin ($\Delta V/V_r$). They concluded that the margin decreases more rapidly when there is finite line resistance compared with the case where zero line resistance is assumed with increasing array size.[55] Lo et al. reported a similar trend in the reading margin for the voltage sensing scheme with a line resistance increase.[30] According to these results, it is quite obvious that the array size can hardly be far larger than several Mbs even if very thick (very low resistance) Cu wires are used. It must be noted, however, that increasing the metal wire thickness is allowed only to a certain extent because extremely thick wires will result in an unaffordable increase in the stacked thickness for 3D CBAs, which will make the deep-etching process for the bit line holes (see Figure 6b) even more challenging. Considering this, the 3D CBAs with a word plane structure have a much higher probability of being adopted in the future memory.

There has not been any report on the actual fabrication of CBA chips using the word plane structure yet. However, Deng et al. reported the modeling work on the influence of the word plane resistance on the device performance using a standard SPICE simulator.[56] The word plane resistance was regarded as rectangular crossing resistance, so the SPICE simulator could handle the problem. They estimated a minimum word plane thickness (Cu) of ≈5 nm, otherwise the plane resistance becomes too high. The minimum SiO_2 thickness separating word planes is ≈6 nm, otherwise the time-dependent-dielectric-breakdown of the dielectric layer cannot be guaranteed, assuming a vertical bit line diameter of 26 nm and an aspect ratio of 30. They also estimated that there would be an 11-fold increase in the integration density when the feature size decreases to 13 nm.[56]

A plausible method to alleviate the issues related to the line resistance is to adopt RS memory cells whose resistances are far larger than the line resistance. For example, on- and off-state resistances of 1 MΩ and 10 MΩ render the whole circuitry of the memory core quite immune to the problems related to the line resistance which shows a maximum value of several kΩ. In fact, Chen et al. reported that the resistance of the on-state in HfO_2-based memory cells could be as high as 1 MΩ when single layer graphene was inserted between the HfO_2 dielectric and TiN electrode whereas the off-state resistance could be maintained at 10 MΩ.[57] However, the high resistance of the memory cells decreases the read current, and, thus, decreases their access speed.

2.8. Correlation between the CBA Structure and the RS Memory Element Characteristics

Not only the reading voltage schemes but also the usable RS characteristics depend on the type of selection device (or vice versa). **Figure 11** summarizes the three typical memory switching *I*–*V* curves that correspond to a) URS, b) bipolar RS (BRS), and c) the switching diode. These data were achieved from a $Pt/TiO_2/Pt$ memory cell, where the TiO_2 layer was grown by an atomic layer deposition method (see Section 2.9 below). Several notable reviews of the materials properties and cell level characteristics of these memory cells are currently available.[58,59] It is most evidently understood that in URS, also regarded as nonpolar RS, set and reset processes occur regardless of the bias polarity, suggesting that a thermally driven fuse-antifuse mechanism is most likely responsible for this memory type. Many transition metal oxides, such as TiO_2, NiO, HfO_2, ZrO_2, and Al_2O_3 as well as a certain polymer show these characteristics.[16,60–67] A purely nonpolar (or purely thermal) mechanism has hardly been reported, however, and even the URS materials are almost always accompanied to a certain degree by the directional motion of the constituent ions,[59] especially during set switching. The performance of bipolar switching memory cells is generally superior to unipolar cells in terms of the switching speed, endurance, and device variability, while it requires a slightly more complicated drive circuitry as well as a smaller memory window. BRS is dominated by the electric-field-driven migration of ions. In oxides, it is mostly related to the lowering and recovery of the Schottky barriers at the working interface of the metal1/insulator/metal2 structure whereas the other interface remains in the quasi-Ohmic

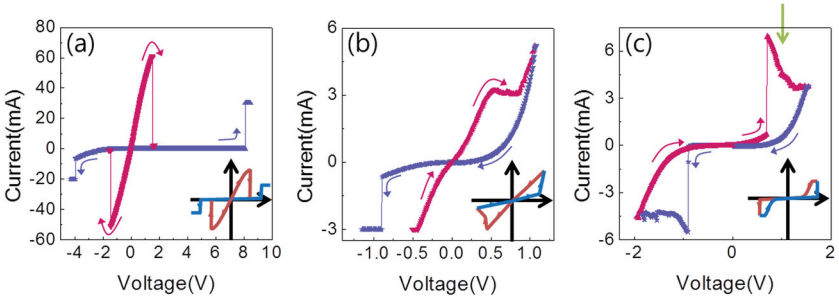

Figure 11. Typical *I–V* curves of a Pt/TiO_2/Pt memory cell in a) URS, b) BRS, and c) switching diode memory modes. The inset figures show schematic *I–V* curves of each mode. BRS and switching diode mode operation could be induced from the URS reset state of the memory cell. Details of transitions between the three modes can be found in ref. [53], [54], and [64].

state. This has usually been observed in asymmetric junction structures such as Pt/Ta_2O_5/TaO/TiN, or in the local region of certain reset-state URS cells, such as Pt/TiO_2/Pt, because of the locally asymmetric configuration of Pt/TiO_{2-x}/Magnéli/Pt in the URS memory cell.[68,69] Electronic BRS based on the trapping and detrapping of electronic carriers that depend on the bias polarity was also reported.[70–72] In an electrochemical-metallization (ECM) cell, such as Cu (or Ag)/solid electrolyte/TiN (or Pt), the active atoms (Cu, Ag) are dissolved into the electrolyte due to a chemical driving force, and are subsequently ionized.[73–76] The electric field drives the positively charged metal ions within the electrolyte to the cathode while the drifted metal ions are reduced at the cathode interface, resulting in a metal bridge (filament). Reversing the electric-field direction first cuts out the weakest part of the metal bridge and in some cases further shrinks the filament during the reset step.[77] Therefore, in this case, the bias polarity obviously drives the set/reset of the memory cell. Several cases where the metal filament growth direction is not consistent with the classical electrochemical theory were recently reported,[78,79] but a rigorous understanding of these peculiar phenomena has yet to be achieved. The occurrence of a switching diode can be understood from a model system where the BRS switching mechanism is extended from one interface to the opposite interface. In the BRS of oxides, oxygen vacancies usually migrate between the active interface and the bulk of oxides (or reservoir of vacancies), depending on the bias direction. In the switching diode, an almost complete sweep of the given amount of oxygen vacancies from one interface to the other, and vice versa, depending on the bias polarity, results in the *I–V* curve shown in Figure 11c.[69,80] The characteristic difference of the *I–V* switching curve of a switching diode from that of a threshold switch, which would serve as a selection device, is described later.

From the view point of the sneak currents, the CBA of the three memory types suffers from read-disturbance if an inappropriate selection device is adopted; in URS and BRS, there are almost always sneak paths consisting of on-state cells. For the switching diode, there is a risk that a number of on-state cells will form a leakage path when the V_r or $-V_r$ scheme is adopted. When the $V_r/2$ or $-V_r/2$ scheme is adopted, the switching diode resembles a self-embedded nonlinear *I–V* device. Therefore, all of these memory cells require the adoption of appropriate selection devices, but the applicable selector types are different for different memory types.

The selection devices can be broadly classified into two groups, as already mentioned earlier: the rectifier and the nonlinear *I–V* device. The rectification property can be well represented by the F/R ratio, which is the ratio between the forward and reverse currents. When considering the sneak path for reading a certain memory cell, all the accompanying sneak paths can be represented by the parallel components R_{s1}, R_{s2}, and R_{s3}, which are serially connected. For the V_r and $-V_r$ schemes, R_{s2} always has a reverse voltage polarity compared with that of the selected memory cell, so that adopting a rectifier can be a viable option for these cases. In these cases, it can be understood that the F/R ratio must be higher than *M* or *N* in Equation (1) to make R_{s2} sufficiently larger than R_{s1} and R_{s3}. When this is the case,

$$R_{st} \approx \frac{R_{diode,rev}}{NM}, \text{and } \frac{R_{diode,rev}}{NML} \tag{3}$$

for 2D and 3D CBAs, respectively.

For the highly nonlinear *I–V* devices, the followings issues must be considered. As can be understood from the equivalent circuit in Figure 2c, one sneak path has a total resistance of $(M-1)R_{s1}+R_{s2}+(N-1)R_{s3}$, and as already discussed above (Table 1), R_{s2} shows zero voltage if there is no voltage drop within the bit and word lines for the $V_r/2$ and $-V_r/2$ schemes. This feature of the two schemes makes the highly nonlinear *I–V* selectors desirable for these cases. When the nonlinear *I–V* selector is adopted, the current through R_{s1}, whose voltage is $V_r/2$ (Table 1), is transferred to the unselected bit lines. When the nonlinearity coefficient, C_{nl}, is defined as the ratio between the currents at V_r and $V_r/2$, the wasted current through each R_{s1} is on-state current/C_{nl}. As there are (*N*–1) of R_{s1}, the total wasted current is $(N-1)$ times higher than this value. In contrast, the current through R_{s3}, which is similarly calculated to be $(M-1)$ on state current/C_{nl}, directly contributes to the sneak current as they flow into the sense amplifier through the selected bit line. Therefore, in order to decrease the power loss (through R_{s1}) and sensing disturbance (through R_{s3}) for high values of *M* and *N*, C_{nl} must be as large as possible. Burr et al. have reported a C_{nl} as high as $\approx 10^7$ from the mixed ionic-electronic conductors (MIEC).[81]

Figure 12 shows schematic *I–V* curves of the typical selection devices: a) unidirectional diode; b) Zener-type bidirectional diode; and c) bidirectional threshold switch. The dotted line in Figure 12b represents a symmetric nonlinear *I–V* device. Before the main discussion on the use of each type of selection device in CBAs is presented, it is worth to briefly address the working principle of each type of selector. Nonlinearity of the *I–V* characteristics of the former two selection devices (a and b) allows to assign the selectivity to the selected cells. Unidirectional diode behavior is observed in not only conventional pn-junction and Schottky diodes but also in capacitor-like back-to-back Schottky diodes.[82] Back-to-back Schottky diodes utilize asymmetric Schottky barrier heights in the capacitors, which can be caused by the use of asymmetric electrodes or

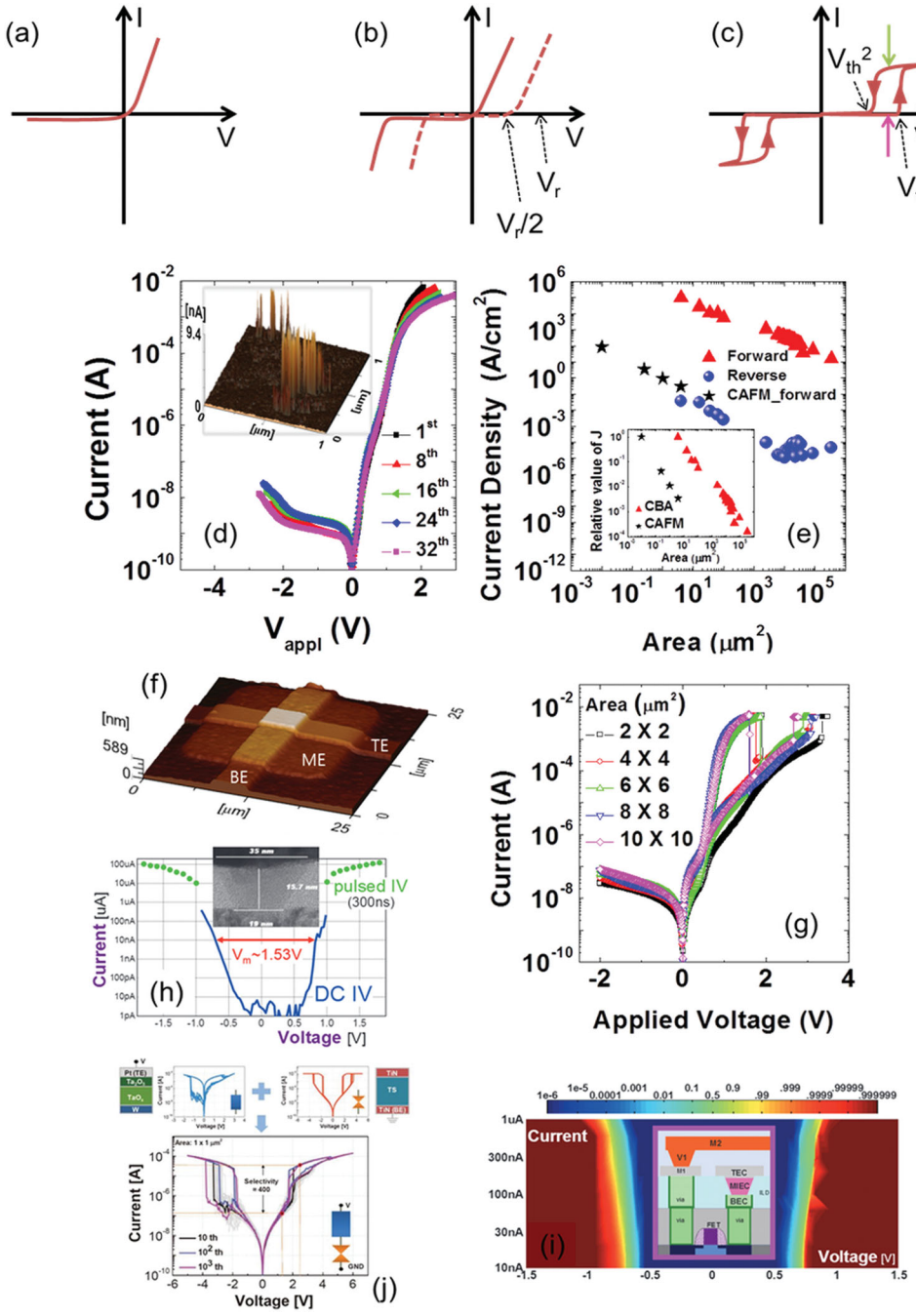

Figure 12. Schematic current–voltage curves of a) a unidirectional diode, b) a Zener-type bidirectional diode, and c) the threshold switch of selectors.The dashed line in (b) represents a highly non-linear *I–V* selector. d) Electrical *I–V* characteristics of a 10×10 μm^2 active area of a crossbar-type Schottky diode whose structure is Pt/TiO_2/Ti/Pt. The inset shows the local current conduction paths in the capacitor-like Schottky diode measured by conductive atomic force microscopy (CAFM). e) Relationship between the current density and active area in both forward and reverse state currents of the crossbar-type and capacitor-like Schottky diode device in (d). The inset shows the relationship between the relative value of the current density and active area in both the CAFM measurement and devices. d,e) Reproduced with permission.[53] Copyright 2012, AIP Publishing LLC. f) AFM image of the fabricated crossbar array device with a top and bottom electrode line width of 4 μm. g) The switching DC *I–V* curves of a stacked Schottky diode/URS Pt/TiO_2/Pt memory cell, studied using a structure of 32×1 type 1D-1R CBA with various line widths (2, 4, 6, 8, and 10 μm). The Schottky diode and Pt/TiO_2/Pt memory cell are separated but electrically connected by adopting a Ni-barrier layer (middle electrode (ME) in Figure (f). f,g) Reproduced with permission.[54] h,i) Representative example of a bi-directional selector, which was reported by the IBM group, using the MIEC-based material.[85] h) High voltage margin (for which leakage stays below 10 nA), high ON current densities, ultra-low leakage (<10 pA), good scalability (<30 nm CD, <12 nm thickness). i) Tight margins (as well as 100% yield) when integrated on 8 inch CMOS wafers in large (512 kBit) arrays. h,i) Reproduced with permission.[85] Copyright 2013, The Japan Society of Applied Physics. j) Bipolar memory switching *I–V* curve of Ta_2O_5/TaO_x (upper left panel) and threshold switching *I–V* curve of AsTeGeSiN sector device (upper right panel). Main panel figure shows the *I–V* curves of the stacked memory and threshold switching devices. j) Reproduced with permission.[86] Copyright 2013, The Japan Society of Applied Physics.

different process conditions for the two Schottky interfaces. In a back-to-back Schottky diode, the Schottky barrier height that electrons in the cathode see when injected from the cathode is different depending on the applied voltage polarity, and thus the *I–V* behavior is largely asymmetric. Theoretical studies on current transport in a back-to-back Schottky diode revealed the importance of the injection current as an overall current-determining conduction contribution when employing a thin insulator.[82,83] In addition, the nonlinear *I–V* behavior is realized by the voltage-dependent change of the Schottky barrier height, which exponentially varies the injection current, i.e., high nonlinearity.[82–84] The voltage-dependence of the Schottky barrier height can arise from, for instance, image charges effects and an interfacial dipole layer at the metal/insulator interface.

Zener-type bidirectional diodes are of symmetric high *I–V* nonlinearity, where the nonlinearity barely depends on the applied voltage polarity. Besides conventional Zener diodes, several capacitor-like bidirectional diodes have been achieved, such as MIEC-based selection devices. The working principle of capacitor-like bidirectional diodes utilizing injection current is straightforward because the nonlinear *I–V* can be realized via the same mechanism as the unidirectional diodes and the symmetry of the *I–V* behavior by the use of symmetric electrodes. Note that the aforementioned MIEC-based selectors are based on both electronic and ionic transport mechanisms, so that the working principle seems to be quite different from the bidirectional diodes utilizing the injection-current.[81]

The essential feature of the threshold switches as selection devices is the transition between two (or more) distinctive resistance states; a stable ground (highly resistive) state and a less resistive state that is only stable when the applied voltage is above a certain threshold, so that the threshold switching is mono-stable.[87] Threshold switching has been observed in VO_2, which is sometimes known to be a Mott-insulator,[27,88,89] and amorphous higher chalcogenides such as GeSe,[90] AsTeGeSi,[91] and AsTeGeSiN.[53,54,85,86] Threshold switching in VO_2, however, has not been clearly understood for the moment, although several mechanisms have been suggested so far. For instance, evolution of high-temperature-induced metallic phases, non-stoichiometric VO_{2-x} phases due to oxygen vacancies, and Magnéli phases have been suggested.[88,89] Mechanisms for threshold switching in the aforementioned amorphous higher chacogenids are not clear as well. So far suggested mechanisms can be classified as a thermal,[92,93] a non-thermal, and a purely electronic model;[94,95] the former accounts for the high resistance state realized by "hot" electrons flowing through electronic conduction channels and the latter for the double-injection of "cold" electrons and "cold" holes. Both mechanisms and their comparison were well addressed in the review paper by Adler et al.[96] Although the Mott-type metal-insulator transition has been suggested as a feasible selector mechanism in several materials, such as VO_2,[27,88,89,97] it is not yet clear whether the change in correlated charge distribution can be utilized as a selector device in CBA.

Data in Figures 12d-j were taken from recent reports on this topic.[53,54,85,86] Figure 12d shows the *I–V* characteristics of a 10×10 μm^2 active area of a crossbar-type Schottky diode whose structure is Pt/TiO_2/Ti/Pt.[53] The inset shows the local current conduction paths in the capacitor-like Schottky diode measured by conductive atomic force microscopy (CAFM). Figure 12e shows the relationship between the current density and active area in both forward and reverse state currents of the crossbar-type and capacitor-like Schottky diode device shown in Figure 12d.[53] The inset shows the relationship between the relative value of current density and active area in both the CAFM measurement and devices. Figure 12f is an AFM image of the fabricated crossbar array device with a top and bottom electrode line width of 4 μm, where the Schottky diode and Pt/TiO_2/Pt memory cell are stacked and the chemical reaction between them is prevented by adopting a Ni-barrier layer (middle electrode (ME) in the figure).[54] Figure 12g shows the switching *I–V* curves of a stacked Schottky diode/URS Pt/TiO_2/Pt memory cell, studied using a structure of 32×1 type 1D-1R CBA with various line widths (2, 4, 6, 8, and 10 μm).[54] Figure 12h,i show the representative example of a bi-directional selector, which was reported by the IBM group.[85] They reported MIEC-based selectors where the migration of active metal (typically Cu) according to the bias resulted in the very high on/off current ratio at V_m and $V_m/2$, where V_m is the voltage where the memory cell is read out. They have reported fully functional CBAs with 512 kbit density over 8-inch wafer, which is a very promising result. Figure 12j shows bipolar memory switching *I–V* curves of Ta_2O_5/TaO_x (upper left panel) and threshold switching *I–V* curves of AsTeGeSiN selection devices (upper right panel) reported by the Samsung group.[86] The main panel of Figure 12j shows the *I–V* curves of the stacked memory and threshold switching devices.[86] Unidirectional diodes generally have high rectification ratios, which have been reported in the pn-junction or Schottky diode.[16–18,20–23] This type of selector is appropriate for the URS memory cell with a very high integration density due to the high rectification ratio and unidirectional current flow. It cannot be used, however, for the BRS-type memory cell as long as the BRS memory requires a high current flow for both set and reset switchings. BRS type memory has generally higher write/erase endurance than URS.[68,98] The Zener-type diode probably works as the selector for the BRS-type memory cell, but this requires a careful tuning of the operation voltage region.[99] In addition, the Zener-type diode usually has an inferior rectification ratio compared with the unidirectional diode, so that this type of selector and memory may constitute lower-density CBAs, but one with a faster switching speed and higher endurance.

Threshold switches have recently been revisited and attracted large attention due to their possible use in CBAs as selection devices.[24,25,27,90,100] Compared with the *I–V* curve of the switching diode shown in Figure 11c, the *I–V* of the threshold switch implies that it can also be used as a memory element, but this is not really the case. For example, if the state of the memory indicated by the green arrow in Figure 11c is checked after the voltage is removed and applied again, it can be seen that the on-state was retained. In contrast, when the same was performed for the state indicated by the green arrow in Figure 12c, the state is changed to a point indicated by the pink (upward) arrow in the same figure corresponding to off-state, meaning that this cannot be used as a memory. Both hysteretic and non-hysteretic nonlinear *I–V* devices require a high current ratio between V_r and $V_r/2$ (Figure 12b). While the understanding of how the non-hysteretic nonlinear *I–V* device should

Table 2. The combinations table of memory and selector. Seven out of nine combinations are possible in principle. Last row indicates the required features of the selector.

	Uni-polar Diode	Bi-polar Diode	Threshold Switch
URS	O	O	O
BRS	X	O	O
SWD	X	O	O
	High rectifying	Rectifying + Nonlinearity	High nonlinearity

be used (designed) as the selector is straightforward, that for the threshold device is quite complicated. As the selector on-state is achieved only after the application of a voltage higher than V_{th1} in Figure 12c, the circuitry for operating such device must be more complicated. Meanwhile, the very abrupt decrease of the conductance at V_{th2} makes it attractive as a highly nonlinear *I–V* selector.[101] The width of the hysteretic curve ($V_{th1} - V_{th2}$) influences the appropriate voltage range for the memory operation. When the width is large, the selector tends to have low resistance near $V_r/2$, meaning that only a small voltage is necessary to maintain a high conductance state. Therefore, the overall voltage necessary to operate the 1selector + 1memory can be low. In contrast, the small width of the hysteretic curve requires a relatively high voltage to maintain the turn-on state of the threshold switch, so that generally a higher voltage is necessary to operate the system. However, a very high endurance, which is the number of possible switching cycles without malfunctioning, is required for the threshold switch, as discussed below. Considering that there are three typical types of memories and selectors, respectively, from the circuit point of view, there could be nine different combinations, as shown in **Table 2**. In principle, only seven cases are possible because the highly unidirectional diode cannot be used for the BRS and switching diode memory. Such limitations originate mainly from the writing operations of each memory type.

According to Table 2, the URS memory can adopt all the three types of selectors, but the thermally driven reactions especially for the memory reset operation generally require a very high current density. Kim et al. already reported that the unipolar diode must have a forward current density of $\approx 10^5$–10^6 A cm^{-2} and a rectification ratio of $\approx 10^6$–10^7.[19]

For the BRS and switching diode memory, the bipolar diode and threshold switches can be adopted, but there are certain discrepancies between the requirements for different types of selectors. For the non-hysteretic selectors, such as the bipolar diode or nonlinear *I–V* device, the maximum voltages that selectors undergo are the turn-on voltage of the selector during the writing, and the turn-on voltage of the selector during reading. For the hysteretic threshold switch, however, for it to be turned on, it must always undergo the peak voltage (see Figure 12c), which is usually much higher than the turn-on voltage necessary for writing and reading, meaning that the endurance test condition for the threshold switch must be harsher.

The complementary resistive switch (CRS) is another class of RS memory cell that is distinct from the other 1T-1R or 1D-1R devices from the operational point of view.[102] It can be composed of any of the known RS materials and does not need to use any selector, but ECM or valence-change-memory (VCM) type bias-polarity-dependent materials are the most well suited systems for this type of configuration.[102,103] CRS is composed of two anti-serially connected BRS cells, whose overall data state depends on which of the two cells is responding to the external stimuli during reading while one of the two cells always remains in off-state (LRS/HRS or HRS/LRS), except during reading, so that it can in principle exclude the sneak current problem. The destructive read-out requiring an exceptionally high endurance and the presence of a voltage-matching series resistor, however, could be the potential problem of this configuration. The off- to on-resistance ratio of the memory corresponds to the F/R ratio of the diodes or C_{nl} of the nonlinear selection devices. As discussed earlier, the unexpectedly high line resistance in the nano-scale CBAs will aggravate this problem of CRS because the CRS memory cells at different locations will have different series resistance values. Meanwhile, an interesting suggestion regarding the role of high series resistance to the RS array based on the nanometallic RS materials was recently reported.[104]

2.9. Processes and Materials for 3D CBA

Fabrication of vertically integrated devices with extremely scaled feature sizes (<20 nm) requires various challenging process steps for photolithography, etching, thin film deposition, and cleaning. This applies not only for the 3D CBAs but also for other vertical devices, such as vertical NAND flash. While the deposition of alternating metal and insulating layers to form the stacked word-planes could be relatively easily accomplished by conventional chemical vapor deposition (CVD) of the insulator (SiO_2) layer and sputtering of the metal layer, the etching of deep holes within the stacked layer for introducing the bit-lines and functional RS layers is a significant challenge for both the dry etching and lithography. Due to the very different chemical reactivity of the insulating and metal layers toward the etching gas chemistry, multiple etching and lithographic processes might be necessary as it is already the case for fabricating the vertical NAND flash devices. Once such steps are completed, the deposition of RS layers, selector layers, and metal wires within the narrow bit-line hole requires thin film deposition processes that possess ≈100% conformality, thickness controllability with atomic-level accuracy, and very large area uniformity. Looking at the promising 3D CBA structure shown in Figure 7b, it can be easily imagined that the allowed thickness for the various metal and oxide layers in the bit-line holes is only a few nanometers when the feature size is < 20 nm. Therefore, thickness control with atomic scale accuracy is indispensable. Such demanding requirements for the film deposition could be met only by atomic layer deposition (ALD).[105,106] ALD has been spotlighted as an important technique for depositing nanometer-scale functional thin films, thanks to its self-limiting surface reaction, which offers atomic-level controllability and unprecedented conformality on extreme three-dimensional surface topologies. Readers are suggested to see the short movie for the functional deposition process of ALD on deep contact hole provided by Cambridge Nanotech.[107] ALD is usually supposed to be applied under

growth conditions where the growing film surface is well saturated with the chemically adsorbing species. Under these circumstances, the growth per cycle (GPC) of the film is constant in each deposition cycle, and the thickness of the film increases linearly with the number of deposition cycles. The ideal ALD reactions of compounds consist of two self-terminating surface reactions of a reactive metal precursor and a reactant gas.[108,109] A model example of ALD with almost perfect self-limited reactions is the formation of Al_2O_3 using $Al(CH_3)_3$ and H_2O.[108] Al_2O_3 is a commonly adopted material in the RS field as the thin insulating barrier layer. This reaction ($2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 6CH_4$) shows an extremely high change in enthalpy due to a very strong bonding energy between Al-O and the high affinity between the CH_3 ligands and H^+ ions.[108] The typical growth rate of Al_2O_3 ALD is ≈0.1 nm/cycle which is approximately one atomic layer thickness/cycle. However, many ALD processes for depositing other functional layers deviate to a different degree from such an ideal ALD reaction due to many reasons. For details about the non-ideal aspects of ALD, see a recent review by Lee et al.[110] Another facile ALD reaction that can produce functional TiO_2 RS materials is the reaction between $TiCl_4$ and H_2O ($TiCl_4 + 2H_2O \rightarrow TiO_2 + 4HCl$), or between $Ti(OC_3H_7)_4$ and H_2O ($Ti(OC_3H_7)_4 + 2H_2O \rightarrow TiO_2 + 4HOC_3H_7$). Sometimes, H_2O is replaced with O_3, which has a stronger oxidation potential than H_2O. The unipolar, bipolar and switching diode-type RS data shown in Figure 11 were achieved from the ALD TiO_2 film using $Ti(OC_3H_7)_4$ and H_2O. Depending on the types of oxygen source for the given $Ti(OC_3H_7)_4$, the resulting microstructure and interface properties are different, which eventually largely influences the RS performance.[111] Other transition metal oxides, such as NiO,[112] ZrO_2,[113] HfO_2,[113] ZnO[114] or doped/undoped perovskite oxides,[110] can be also grown by ALD. The excellent step coverages of these RS oxides in a small-diameter contact hole structure have been confirmed.

Another promising deposition method for oxide films is the supercritical fluid deposition. Jung et al. reported the TiO_2 film deposition using the supercritical fluid deposition method with a step coverage of >97% on a contact hole with an aspect ratio of 50.[115]

In contrast, there are several material classes which are generally difficult to be processed by ALD. Phase changing (sometimes threshold switching or even resistance switching) chalcogenides, such as Ge-Sb-Te compounds, and elemental metals used as electrode materials, such Ru, are one of the examples. Although the Ge-Sb-Te compounds are the primary candidate for the phase change memory, it has been adopted in vertical RRAM-type devices recently utilizing a NAND-like chain architecture (vertical chain-cell-type phase change memory (VCCOCM)).[116] While several previous reports mostly adopted the CVD-like behaviors of metal-organic precursors,[117–119] a genuine ALD of $Ge_2Sb_2Te_5$ was reported only recently by Pore et al.,[120] which has been hindered by the lack of an appropriate chemical-reaction route for the ALD-type reaction. The innovative improvements made in that report are due to the strong Lewis acid-base reaction between the ligands of the silyl-Te (ethylsilyl group in $((C_2H_5)_3Si)_2Te$) and $GeCl_2$·dioxane complex, and various alkoxides of Sb. The highly viable chemical reaction of the Ge- and Sb-precursors toward the Te-precursor allowed the ALD reaction to take place at a substrate temperature as low as 60 °C.[120] Adopting the idea of utilizing the Lewis acid-base reaction of the silyl-Te and volatile precursors of Ge and Sb ($Ge(OCH_3)_4$ and $Sb(OC_2H_5)_3$), some of the authors also recently reported ALD of materials with compositions lying on the tie line between $GeTe_2$ and Sb_2Te_3, such as $Ge_2Sb_2Te_7$.[121] The occurrence of the $GeTe_2$ component was mainly ascribed to the +4 oxidation state of the Ge ions in the Ge precursor. $Ge_2Sb_2Te_7$ showed a fluent phase change and accompanying resistance change properties comparable to those of $Ge_2Sb_2Te_5$. **Figure 13**a–d show the high performance of the ALD process resulting in conformal $Ge_2Sb_2Te_7$ thin films and contact filling properties of the same material at a substrate temperature of 70 °C. Not only the thickness but also the uniformity of the chemical compositions is confirmed.

Along with the ALD of these functional RS or selector layers, metal electrodes (bit-line in Figure 7) must be also grown by ALD. ALD of metal is generally more challenging compared with that of compounds due to the lack of facile ALD reaction routes for many metals. Development of metal ALD has been invoked by the DRAM capacitor electrode (Ru, RuO_2, $SrRuO_3$),[123–125] and back end of the line process of logic chip fabrication containing materials such as W, Ru, Cu, and TiN or TaN.[126] Among these materials, TiN and TaN are the barrier and electrode material for the switching layer, and could be readily deposited by ALD using facile chemical reaction routes such as $6TiCl_4 + 8NH_3 \rightarrow 6TiN + 24HCl + N_2$, and $3TaCl_5 + 5NH_3 \rightarrow 3TaN + 15HCl + N_2$. ALD of noble metal, such as Ru, could be reasonably well achieved by the oxide deposition and subsequent reduction at each ALD cycle. One of the examples showing the excellent conformality of ALD Ru film in deep contact hole is given in Figure 13e.[122]

CVD W can be used to fill the deep contact holes and vias on account of its good step coverage and relatively easy processing based on the reduction of WF_6 source gas by H_2 or SiH_4.[127,128] With the smaller and deeper contact holes as shown in Figure 7 for vertical 3D CBA, the step coverage of CVD W process becomes insufficient. In particular, the seed layer (or nucleation layer) growth step with a lower deposition rate but better conformality suffers from the inadequate step coverage in highly scaled devices. Therefore, an ALD W process for replacing the nucleation CVD W step is under development.[129,130]

ALD of Cu has been reported to be challenging although several ALD reaction route has been suggested. There are numbers of Cu-precursors, such as copper(I) monochloride [$(CuCl)_3$], β-diketonate derivatives, copper (II) bis(2,4-pentanedionate) [Cu(acac)2], copper bis(2,2,6,6-tetramethyl-3,5-heptanedionate) [$Cu(thd)_2$], copper(II) hexafluoroacetylacetonate hydrate [$Cu(hfac)_2 \cdot xH_2O$], and copper (I) amidinate of N,N′-di-iso-propylacetamidinato copper(I) [Cu (iPr-amd)$_2$], have been reported.[126] Most of these are reduced by thermal H_2-gas or plasma-enhanced H_2 gas during the ALD of Cu. However, some of the precursors are not sufficiently thermally stable at bubbling temperature, and some other precursors produce Cu films with relatively high concentration of impurities. However, there are several promising ALD results of Cu making its adoption to 3D CBA feasible.[131,132] Detailed review for these metals could be found in ref. [126].

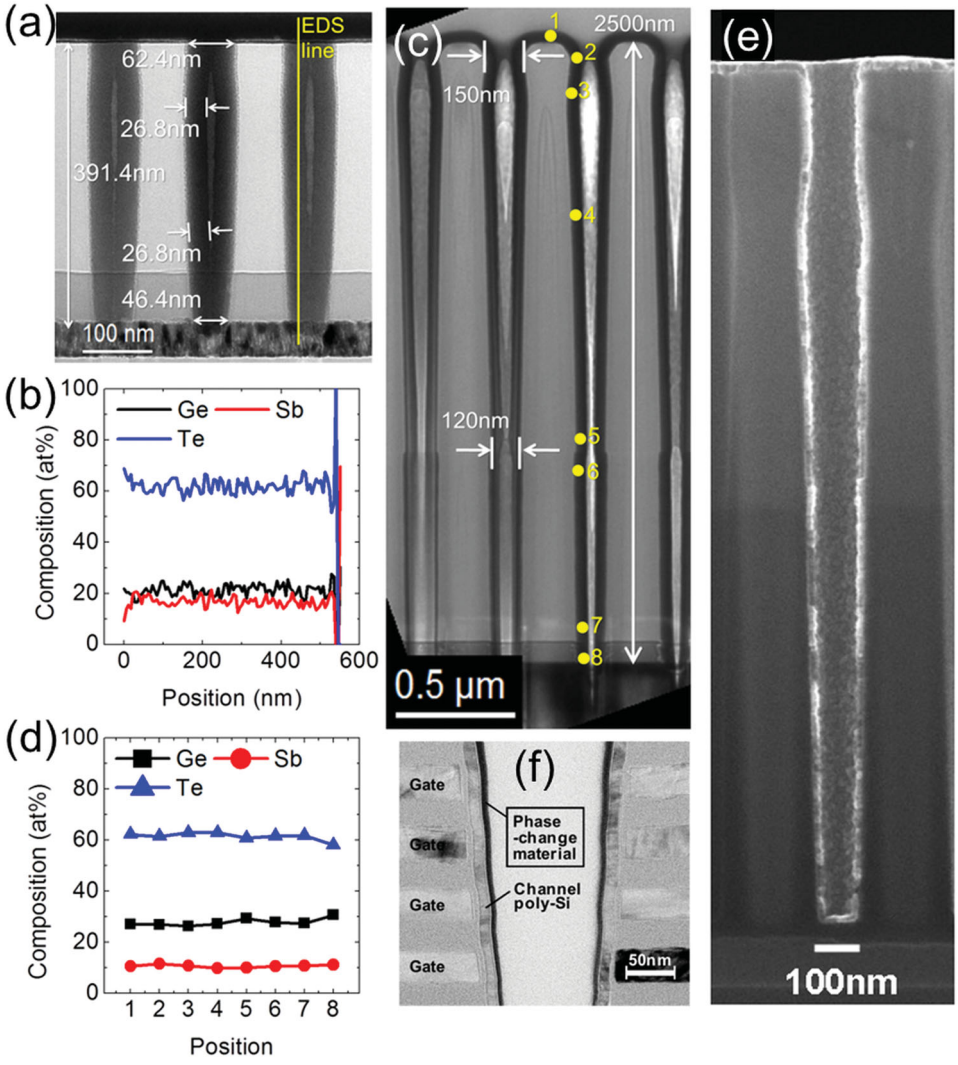

Figure 13. Cross-section transmission electron miscroscopy (TEM) images showing the conformal deposition of $(GeTe_2)_{0.66}(Sb_2Te_3)_{0.33}$ film on contact hole. a) Completely filled contact hole with the TiN interfacial layer when $n_{cy}^{s} = 200$. b) Energy dispersive spectroscopy (EDS) line profile of the three elements along the line shown in (a). c) Cross-section TEM image of the $(GeTe_2)_{0.66}(Sb_2Te_3)_{0.33}$ film ($n_{cy}^{s} = 60$) on the contact hole with an aspect ratio of 20. d) EDS profile of the three elements along the $(GeTe_2)_{0.66}(Sb_2Te_3)_{0.33}$ in the side wall of the hole marked by numbers in c). a–d) Reproduced with permission.[121] Copyright 2012, American Chemical Society. e) Cross-section SEM image of contact hole having conformal Ru layer deposited by ALD using 2,4-(dimethylpentadienyl)(ethylcyclopentadienyl)Ru as the Ru-precursor. e) Reproduced with permission.[122] Copyright 2007, The Electrochemical Society. f) Cross-section of vertical chain-cell-type phase change memory. f) Reproduced with permission.[116] Copyright 2012, IEEE.

The generally quite slow growth rate (GPC) of ALD will not be a critical problem for 3D CBA as the required thickness of each ALD layer is pretty small (≈several nm).

So far, there have been only handful of reports which rigorously utilized the genuine ALD processes to make the vertical 3D CBA devices.[32–36] However, it is highly expected that many more report will soon appear as there is no other feasible way for fabricating the technically viable 3D CBA without adopting the ALD processes. Figure 13f shows a cross-section image of VCCPCM. In this architecture, a NAND-like chain architecture was accomplished achieved by combining the conventional vertical MOSFET technology with vertically integrated phase change material.[116]

There are many other process related issues such as fine patterning (lithography) and anisotropic etching of deep holes and trenches for vertical CBA, and thin metal wires for 2D CBA. Especially, the hyper-fine patterning of metal wires, of which thickness could be much thicker than their width, to ensure the low enough wire resistance, should not be a trivial task even in the 2D CBA devices. Etching of deep holes for the 3D CBA fabrication is highly challenging which is already well known in the fabrication of vertical NAND flash. The extremely high aspect ratio of the deep holes may not allow the plasma etching gas to reach the bottom area of the hole, stopping the etching while the masks are kept eroding. Subdividing the many layers into two or three groups, and repeated photo-etching processes

might be necessary if one requires a very large number of stacked layers.

2.10. Other Problems of the 2D and 3D CBAs

Even though the 2D and 3D CBAs have a high potential to be adopted as the next-generation high-density memories, and even though many methods have been suggested for their fabrication, as summarized in Table 1 and 2, when viewed from the view point of the rather idealized circuitry, there are several crucial materials and process problems remained. Such problems actually become even worse as the device size shrinks further. In this section, several representative problems are discussed, but this does not necessarily imply that these are the only significant problems.

The issues related to the bit and word line resistances have already been discussed in Section 2.7. Here, the problem is shortly revisited. Kim et al.[29] reported that the reset and set voltages that need to be applied ($V_{a,reset(set)}$) when the line resistance is not negligible can be represented by Equation (4).

$$V_{a,reset(set)} = V_{reset(set)}\left(1+\frac{R_{line}}{R_{LRS(HRS)}}\right) \quad (4)$$

where $V_{reset(set)}$, R_{line}, and $R_{LRS(HRS)}$ are the reset (set) voltage, line resistance, and resistance of the memory cell in LRS (HRS), respectively. As $R_{LRS} << R_{HRS}$, V_{reset} increases faster than V_{set} with increasing R_{line}, and eventually, $V_{reset} > V_{set}$ at a certain R_{line} value. This is a catastrophic situation, where HRS cannot be obtained in URS, and such restriction can be readily applied in array device fabrication with nm scale. For example, when Cu wires with a width and a thickness of 20 (F = 20 nm) and 100 nm, respectively, are used as the bit and word lines, and when the URS memory with R_{LRS} of 60 Ω, R_{HRS} of 6000 Ω, V_{set} of 2 V, and V_{reset} of 1 V is used, R_{line} must be ≤61 Ω assuming the bulk conductivity of Cu. This means that the maximum 2D CBA size is only 100×100, which is unreasonably small. Even worse, the difference in actual voltage between the cells close to and far from the voltage source can no longer be ignored. These problems must be solved only by decreasing the line resistance or increases the memory cell resistance significantly. However, a too high memory cell resistance accompanies with a problem of too slow speed of operation.

Thermochemically driven RS devices as well as electric-field-driven VCM devices require a quite high current to write data, especially during reset operation. Even though there have been several works reporting an extremely small operation current (only several μA) or power (several tens of pW),[133,134] the typical oxide-based RRAMs require several tens to hundreds μA, with the electrode area down to 100×100 nm^2.[135–137] This is in fact a quite harsh condition for the selection device, which must offer an extremely high forward current density (≈10^5–10^7 A cm^{-2}) and an extremely high rectification ratio (≈10^6–10^7) at the same time.[19,24,28,81] It must be noted that electromigration starts to occur at a current density of ≈10^6–10^7 A cm^{-2} in Cu.[138] Thus, there is not much room for a substantial increase in array density.

Fabricating CBAs during the back-end of the line of Si wafer processing is expected to be accomplished by the general process steps in the CMOSFET lines. It is expected that the most critical fabrication step for 2D CBA is fine-line patterning. The cross-line patterning of metal wires (Pt and Cu) with a tens of nanometer width has been reported by the nano-imprint technology,[139,140] with a certain limited density. This will eventually be replaced with the standard deep ultraviolet lithography and reactive ion etching techniques. The functional RS layers as well as electrode layers could be deposited via atomic layer deposition (ALD) considering its atomic-scale accuracy in film control that will be ultimately required. The capacitive coupling between the parallel metal lines must also be considered, which has not yet been seriously dealt with. If the line thickness increases due to the reasons mentioned above, such coupling will become severer and will decrease the device speed and sometimes induce malfunction.

For 3D CBAs, the structure shown in Figure 7b may have the highest feasibility considering the fabrication processes. For the other structure (Figure 7a), it may be too difficult to make numerous free-standing metal nanowires for bit lines. After making the holes in the stacked word planes and insulating layer, see Figure 7b, the functional layers must be deposited conformally over the seriously deep and narrow holes, which would make the use of the ALD technique inevitable, as described in detail in Section 2.9. If the memory and selection device layers are all insulators and conduct electricity between the word plane and vertical bit lines depending only on the memory states, the fabrication step can be simple: depositing the memory/selector layers via ALD and filling out the remaining hole space via metal ALD, which would be the bit lines. If any metal layer must be sandwiched between the memory and selector layers to realize the necessary memory and selector functionality, however, there will be a problem in laterally etching the vertically coated metal layers to separate the memory cells located vertically. Therefore, the memory and selector must lack intervening metal layers, as shown in **Figure 14**a. In the report on the stacked 1D-1R with a 2D CBA configuration, Kim et al. had to adopt the stacked intermediate metal layers (Pt/Ni) to make the Schottky diode on the top and the metal-insulator-metal configuration of the memory at the bottom, and to prevent oxygen diffusion from the memory to the diode layer.[54] Such a structure, therefore, can hardly be accepted in 3D CBAs even if the ALD processes for all the layers are developed. Therefore, the 1D-1R structure will undergo changes, as shown in Figure 14a.

The I–V curves shown in Figure 14b,c, which were achieved from the Pt/Al_2O_3/NiO/W, and Pt/TiO_2/HfO_2/TiN structures, respectively,[141,142] are very intriguing with regard to the formation of the CBA structure shown in Figure 7b. These I–V curves show a highly improved behavior (Pt/TiO_2/HfO_2/TiN) and a nonlinear progression as well as rectifying properties (Pt/Al_2O_3/NiO/W), in addition to the self-embedded RS performance in the positive voltage region. In recent studies, a similar observation has been reported.[143–145] While the precise understanding of what accounts for such self-rectifying and memory functionalities in a single sample has yet to be achieved, this is a highly promising result considering that all the insulating layers are grown via ALD, which is inevitable for the 3D CBA fabrication.[146,147]

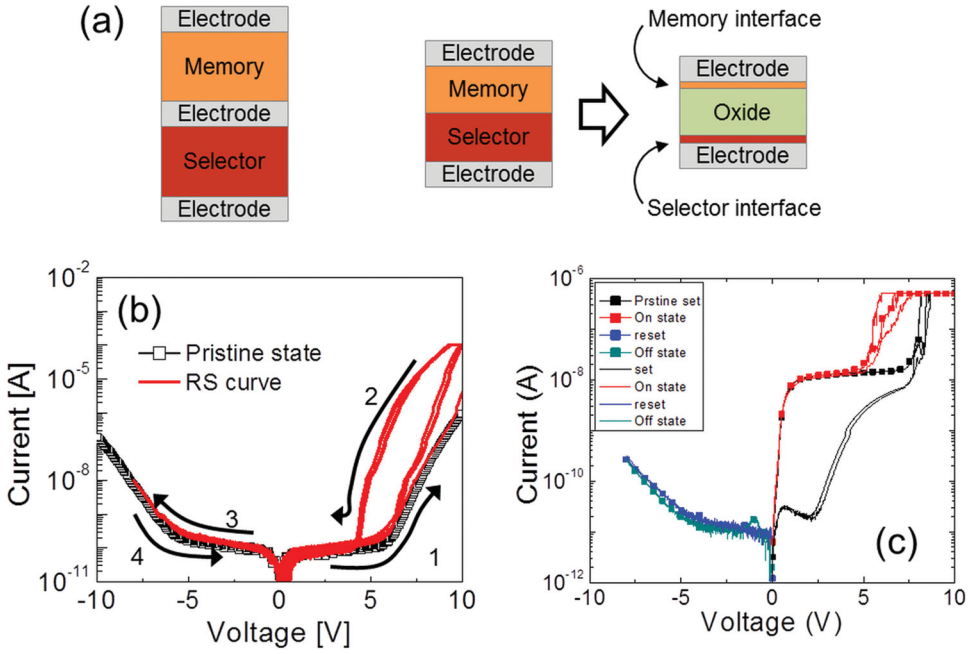

Figure 14. a) Schematic representation of the evolution of 1D-1R structure. *I–V* curve of b) $Pt/Al_2O_3/NiO/W$, and c) $Pt/TiO_2/HfO_2/TiN$ structure. Both *I–V* curves show the self-rectifying behavior, where the current level in negative bias remained very low while the current in the positive voltage side shows fluent resistance switching. The low current in the negative voltage regions in (b) and (c) could be commonly ascribed to high Schottky barrier at the Pt/oxide interface which maintains intact configuration irrespective of memory states shown in positive voltage region. Studies on the detailed mechanism for such peculiar behavior of the material stack are in progress.

The required specification for the self-rectifying CBA depends on the specific design, voltage scheme, and intended array size. However, there is no specific reason why the self-rectifying CBA has different specifications than stacked selector-one resistor devices. The self-rectifying CBA just lacks the intermediate electrode, which has little relevance for the ON resistance and non-linearity.

3. Summary and Outlook

In this article, the impressive improvements in the theoretical understanding and integration of the RS memory with various CBA configurations made in the past decade are summarized. The authors attempted to provide two important quantitative guidelines for the memory integration with respect to the required number of interconnection wires and sneak current paths. The number of interconnection lines (also bit and word lines) in 3D CBAs is generally larger compared with that in 2D CBAs, which undermines the merit of cell area saving by 3D stacking. In addition, the complicated and long interconnection wire layout to the periphery circuits and the increased number of periphery circuits with an increasing number of stacked layers decreases the overall gain in the packing density of 3D CBAs. As the number of total memory cells per memory block increases far higher than several tens of Mb, however, such circuit overhead can be well compensated by cell area saving. Another crucial advantage of 3D CBAs is the shortening of bit and word lines and the accompanying decrease in line resistance, which can be a significant problem in 2D CBAs. If a stacking technology for the periphery circuits can be successfully developed, the primary merit of 3D CBAs (cell area = $4F^2$/stacking number) will be further strengthened. Even in 3D CBAs, there can be several modifications of stack structures, making this field engineering-rich. The alternative stacking of word planes and insulating layers with vertical bit lines in it appears to be the optimum structure for 3D CBA, without sacrificing the simultaneous access of multiple bit lines via the use of multiple bit line decoders. The layer decoder further decreases the space overhead for the peripheral circuits but sacrifices the parallel accessibility.

The extremely parallel and passive geometry of CBAs generally results in a sneak current problem during reading operation. There are several voltage application schemes for minimizing this problem, but they can be duly classified into the V_r and $V_r/2$ schemes. Here, the three typical RS memory types with respect to the voltage application for switching (URS, BRS, and switching diode) are explained. The three typical selection device types for suppressing the sneak current (unidirectional diode, bidirectional diode, or highly nonlinear *I–V* device, and threshold switch) are also discussed. Therefore, there could be fundamentally nine different combinations for the memory and selection devices, and among them two are not usable. The usefulness of the remaining seven combinations is carefully examined for the different voltage application schemes. In general, diode-type selectors are appropriate for the V_r schemes while threshold or nonlinear *I–V* devices with bidirectionality are suitable for the $V_r/2$ schemes.

Several critical issues remain in the material properties of the memories and selectors for the high integration density of CBAs: the high bit and word line resistance, which interferes with the set and reset operations; the maximum affordable

current density by the selector and metal lines; and fabrication process issues. These problems will become highly serious as the device dimension scales to <10 nm. Even though there have been several reports on the RS performance of some materials with a device size <≈50 nm,[133] an RS memory with a rigorous sub-10-nm-scale dimension has not yet been reported. In this memory size range, the present understanding on the nature of RS, such as the conducing filament formation and rupture, may not be applied because the size of the cell is already comparable to the filament dimension. Even worse for this level of memory scale is that not much is known about the possible issues related to the parasitic components, such as the wire resistance, the capacitance of the memory cell, and the capacitive coupling between the wires and planes. Area scaling for the selectors may induce problems related to the maximum available drive current when the current flows uniformly across the device area, which is the case for Si-diodes. As almost all of the resistance switching element possesses a localized current flow, the switching current may not scale as much as the area-type selector does. Therefore, having a low operation current of the memory cell becomes even more important under such circumstances. For poly-crystalline materials being used for any type of selector devices, the problem of cell-to-cell non-uniformity, probably due to the presence of grain boundaries, becomes aggravated when the cell size becomes comparable to the grain size. This is also the case for the memory element. Considering the backend of the line location of the memory cell and selectors in the integrated structure, which prohibits the adoption of epitaxial layers, this type of non-uniformity problem might be minimized when amorphous materials are used. Another aspect of these problems, however, could be that these uncertain factors lead to increased research activities in this field both in academia and industry. Combining the top-down-type research trend of the mainstream RS field with the bottom-up-style research for other nano-engineering fields presents an interesting research topic in the future. It might be an interesting task to make carbon-nanotube (CNT)-based RS cells (i.e., using CNTs as the electrode for the RS memory), and to examine its functionality for ultimate scalability. In fact, this task has been already attempted independently by the researchers in Stanford and Illinois universities, and the results were quite promising although they remained at rather preliminary level yet.[148,149]

This field, or any other high-density non-volatile memory, will eventually find an intriguing application in the neuromorphic research area as the human brain is a big mass of memory as well as non-Boolean logic circuits. Several recent articles explore the application of RS memory in this field,[150,151] but looking back, such a trend can also be found in the ferroelectric research.[152] It seems that the main problem in this field is that it is still not precisely known how the human brain works, and, thus, have not yet determined the direction in which the research field should go.[153]

A different RS research trend can be found in the work on materials implication (IMP) logic reported by the Hewlett Packard Group.[154] This is a completely different way of viewing the logic circuit; the present logic is based on the transfer of logic data in the spatial dimension, but IMP is a logic circuit based on the transfer of logic data in the temporal dimension. Therefore, there must be a revolutionary change in viewing the logic circuits, but CBA can play a crucial role in this field because the configuration of the IMP circuit is basically identical to that of CBA. When a fully functional memory with ultra-low power consumption, perhaps several hundred times smaller than the present memories, is accomplished by fabricating 3D CBA, the data-centric computation would be possible. This will open up a new era of computers.

Acknowledgements

This study was supported by the Global Research Laboratory Program (2012040157) through the National Research Foundation (NRF) of Korea.

Received: October 14, 2013
Revised: March 19, 2014
Published online: July 3, 2014

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